

Contains pages for the

Maintenance Manual

for

AM/FM SIGNAL GENERATOR

2023

&

2024

9 kHz - 1.2 GHz

9 kHz - 2.4 GHz

**Part number 46882-245M
Issue 3**

Creation date 8-Sep-98

Please open and fit to the supplied Ring Binder

AM/FM SIGNAL GENERATOR

2023 & 2024

9 kHz - 1.2 GHz

9 kHz - 2.4 GHz

Includes information on:

- Option 1: No attenuator.
- Option 2: DC operation.
- Option 3: High power.
- Option 4: High stability frequency standard.
- Option 5: Rear panel connectors.
- Option 7: Fast pulse modulation.
- Option 10: 1 V peak mod input.
- Option 11: Fast pulse and high power.
- Option 100: Internal pulse generator.

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Issue 3

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About this manual

This manual provides servicing information to a defined circuit area for the 2023 & 2024 AM/FM Signal Generators.

Intended audience

The book is intended for qualified service engineers and assumes a knowledge of the instrument to a level covered in the Operating Manual 46882-225U.

Structure

Chapter 1 Technical description

This includes block diagrams and detailed board circuit descriptions. The circuit descriptions refer directly to the servicing diagrams contained in Chapter 7.

Chapter 2 Maintenance

Refer to this chapter for board and unit access, service policy and routine safety testing and inspection.

Chapter 3 Adjustment procedures

Refer to this chapter for information on password use and adjustment procedures.

Chapter 4 Initial repair

What to do if the instrument shows no signs of life.

Chapter 5 Fault diagnosis

Based on error message reports and narrows the search down to a defined circuit area.

Chapter 6 Replaceable parts

Contains instrument and board component parts and a section on miscellaneous mechanical parts.

Chapter 7 Servicing diagrams

Contains interconnection drawings, board circuits and component layout diagrams.

Associated publications

Refer to the Operating Manual 46882-225U for an up-to-date list of associated publications.

Contents

Precautions.....	iv
Précautions.....	vii
Vorsichtsmaßnahmen.....	ix
Precauzioni.....	xi
Precauciones.....	xiii
Chapter 1 TECHNICAL DESCRIPTION.....	1-1
Chapter 2 MAINTENANCE.....	2-1
Chapter 3 ADJUSTMENT PROCEDURES.....	3-1
Adjustments.....	3-4
Recommended test equipment.....	3-7
Adjustment procedures.....	3-8
Adjustment procedures for instruments fitted with Option 3 or 1L.....	3-22
Adjustment procedure tables.....	3-24
Appendix A Calibration GPIB commands.....	A-1
Chapter 4 INITIAL REPAIR.....	4-1
Chapter 5 FAULT DIAGNOSIS.....	5-1
Chapter 6 REPLACEABLE PARTS.....	6-1
Chapter 7 SERVICING DIAGRAMS.....	7-1
Circuit notes.....	7-2

Precautions

WARNING

CAUTION

Note

These terms have specific meanings in this manual:-

WARNING

Information to prevent personal injury.

CAUTION





Information to prevent damage to the equipment.

Note

Important general information.

Symbols used on this product

The meaning of hazard symbols appearing on the equipment is as follows: -

Symbol	Nature of hazard
	General hazard
	Dangerous voltage
	Toxic hazard
	Static-sensitive components

General conditions of use

This product is designed and tested to comply with the requirements of IEC/EN61010-1 'Safety requirements for electrical equipment for measurement, control and laboratory use', for Class I portable equipment and is for use in a pollution degree 2 environment. The equipment is designed to operate from an installation category 1 and 2 supply.

Equipment should be protected from the ingress of liquids and precipitation such as rain, snow, etc. When moving the equipment from a cold to a hot environment, it is important to allow the temperature of the equipment to stabilise before it is connected to the supply to avoid condensation forming. The equipment must only be operated within the environmental conditions specified in Chapter 1 'Performance data' in the Operating manual, otherwise the protection provided by the equipment may be impaired.

This product is not approved for use in hazardous atmospheres or medical applications. If the equipment is to be used in a safety-related application, e.g. avionics or military applications, the suitability of the product must be assessed and approved for use by a competent person.

WARNING



Electrical hazards (AC supply voltage)

This equipment conforms with IEC Safety Class I, meaning that it is provided with a protective grounding lead. To maintain this protection the supply lead must always be connected to the source of supply via a socket with a grounded contact.

Be aware that the supply filter contains capacitors that may remain charged after the equipment is disconnected from the supply. Although the stored energy is within the approved safety requirements, a slight shock may be felt if the plug pins are touched immediately after removal.

Fuses

Note that the internal supply fuse is in series with the live conductor of the supply lead. If connection is made to a 2-pin unpolarized supply socket, it is possible for the fuse to become transposed to the neutral conductor, in which case, parts of the equipment could remain at supply potential even after the fuse has ruptured.

Removal of covers

Disconnect the supply before removing the covers so as to avoid the risk of exposing high voltage parts. If any internal adjustment or servicing has to be carried out with the supply on, it must only be performed by a skilled person who is aware of the hazard involved.

WARNING



Fire hazard

Make sure that only fuses of the correct rating and type are used for replacement.

If an integrally fused plug is used on the supply lead, ensure that the fuse rating is commensurate with the current requirements of this equipment. See under 'Performance data' in Chapter 1 in the Operating/Instruction manual for power requirements.

WARNING



Toxic hazards

Some of the components used in this equipment may include resins and other materials which give off toxic fumes if incinerated. Take appropriate precautions, therefore, in the disposal of these items.

WARNING



Beryllia

Beryllia (beryllium oxide) is used in the construction of the following components in this equipment :

TR808 on AA1;
TR1 and TR2 on AA2/1 and AA2/7.

This material, when in the form of fine dust or vapour and inhaled into the lungs, can cause a respiratory disease. In its solid form, as used here, it can be handled quite safely although it is prudent to avoid handling conditions which promote dust formation by surface abrasion.

Because of this hazard, you are advised to be very careful in removing and disposing of these components. Do not put them in the general industrial or domestic waste or despatch them by post. They should be separately and securely packed and clearly identified to show the nature of the hazard and then disposed of in a safe manner by an authorized toxic waste contractor.

WARNING



Beryllium copper


Some mechanical components within this instrument are manufactured from beryllium copper. This is an alloy with a beryllium content of approximately 5%. It represents no risk in normal use.

The material should not be machined, welded or subjected to any process where heat is involved. It must be disposed of as "special waste".

It must NOT be disposed of by incineration.

CAUTION

Static-sensitive components

The presence of static-sensitive components is indicated in the equipment by yellow disks, flags or labels bearing the symbol . Certain handling precautions should be observed to prevent these components being permanently damaged by static charges or fast surges:-

1. If a static-sensitive component is to be removed or replaced, the following anti-static equipment should be used:-
 - A **work bench** with a grounded conductive surface.
 - **Metallic tools** grounded either permanently or by repeated discharges.
 - A **low-voltage** grounded soldering iron.
 - A **grounded wrist strap** and a conductive **grounded seat cover** for the operator whose outer clothing should not be of man-made fibre.
2. If a printed board containing static-sensitive components (as indicated by warning disk or flag) is removed, it must be temporarily stored in a conductive plastic bag.
3. As a general precaution, avoid touching the leads of a static-sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.
4. If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

Chapter 1

TECHNICAL DESCRIPTION

Contents

Introduction	1-4
Synthesiser	1-4
RF processing	1-4
LF processing	1-7
LF output	1-7
AM and level control	1-7
FM/φM	1-7
RF board - AA1	1-8
Carrier frequency synthesis	1-8
RF board: Carrier generation (AA1 sheet 1)	1-8
RF board: VCXO loop (AA1 sheet 2)	1-9
100 MHz VCXO	1-9
100 MHz phase locked loop	1-9
RF board: Synthesiser (AA1 sheet 3)	1-10
Synthesiser operation	1-10
1-bit A-D converter	1-10
RF board: Loop filter and autocal (AA1 sheet 4)	1-11
Loop filter	1-11
Autocalibration	1-12
AA2 board identification	1-12
Power amp cal comparator	1-13
RF board: FM drive (AA1 sheet 5)	1-13
Operation	1-13
RF board: Level modulator (AA1 sheet 6)	1-14
Amplitude modulator	1-14
PIN modulator	1-14
Peak detector and control loop	1-15
Level modulator	1-15
Output unlevelled	1-15
Pulse modulation drive	1-15
RF board: Frequency generator (AA1 sheet 7)	1-16
Frequency generation	1-16
Frequency band selection	1-16
Fundamental octave	1-17
600 MHz to 1.2 GHz generation	1-17
Programmable divider	1-17
RF board: Interface and attenuator drive (AA1 sheet 8)	1-18
Serial bus interface	1-18
Attenuator drive	1-18
Pulse modulation	1-19
RPP control	1-19
High power amplifier option	1-19
RF board: output amplifier (AA1 sheet 9)	1-19
Output amplifier	1-19
BFO-band frequency generation	1-19
RF levelling detector	1-20
ALC loop	1-20
Offset trim	1-20
RF board: Power supplies (AA1 sheet 10)	1-20
Power supplies	1-20

contd./...

TECHNICAL DESCRIPTION

Contents (continued)

Attenuator board - AA2	1-20
Circuit functions	1-20
Pulse modulation	1-21
Attenuator	1-21
Reverse power protection	1-21
High power attenuator board - AA2/1	1-22
Circuit functions	1-22
High power attenuator board: Pulse mod & attenuator (AA2/1 sheet 1)	1-22
Pulse modulation	1-22
Attenuator	1-22
High power attenuator board: Power amp & RPP (AA2/1 sheet 2)	1-23
Power amplifier	1-23
Reverse power protection	1-23
Signal output board - AA2/2	1-24
Circuit function	1-24
Fast pulse modulator board - AA2/5	1-24
Circuit functions	1-24
Fast pulse modulator board: Pulse mod (AA2/5 sheet 1)	1-24
Pulse modulation	1-24
Amplifier	1-25
Fast pulse modulator board: RPP and atten (AA2/5 sheet 2)	1-25
Step attenuator	1-25
Reverse power protection	1-25
Fast pulse and high power board - AA2/7	1-26
Circuit functions	1-26
Fast pulse and high power board: Pulse mod (AA2/7 sheet 2)	1-26
Pulse modulation	1-26
Amplifier	1-26
Fast pulse and high power board: Attenuator (AA2/7 sheet 3)	1-26
Attenuator	1-26
Fast pulse and high power board: Power amp & RPP (AA2/7 sheet 4)	1-27
Power amplifier	1-27
Reverse power protection	1-27
Control board - AB1	1-28
Introduction	1-28
Control board: Microprocessor and memory (AB1 sheet 1)	1-28
Microprocessor	1-28
Interrupts	1-29
Memory bank	1-30
Data transfer	1-30
Control board: DSP audio generator (AB1 sheet 2)	1-31
Trigger	1-31
Pulse modulation	1-32
Control board: Interrupts and serial interface (AB1 sheet 3)	1-32
Interrupt handler	1-32
Serial bus	1-32
Buffered data bus and control lines	1-33
Control board: Modulation and level (AB1 sheet 4)	1-34
External modulation input	1-34
Composite modulation	1-34
Amplitude modulation	1-34
Frequency/Phase modulation	1-34
Control board: Standard selection (AB1 sheet 5)	1-35
Clock circuitry	1-35
Control board: Interface (AB1 sheet 6)	1-36
GPIB	1-36
RS-232	1-36

Knob	1-36
Key pad.....	1-37
Front panel display.....	1-37
Control board: PSU filtering and regulation (AB1 sheet 7).....	1-37
Processor reset.....	1-38
Control board: Power supplies (AB1 sheet 8)	1-38
Power supplies	1-38
Backlight inverter board - AC1	1-39
Front panel - AF1.....	1-39
AC power supply.....	1-39
AC/DC power supply	1-39

List of figures

Fig. 1-1 Signal generator block schematic.....	1-5
Fig. 1-2 100 MHz phase locked loop.....	1-9
Fig. 1-3 Frequency synthesis	1-11
Fig. 1-4 FM/φM drive.....	1-14
Fig. 1-5 Frequency band selection	1-17
Fig. 1-6 Microprocessor and control block diagram.....	1-29
Fig. 1-7 Frequency standard selection	1-36
Fig. 1-8 Block diagram of AC/DC power supply module.....	1-40

List of tables

Table 1-1: Carrier generation	1-8
Table 1-2: Attenuator board identification	1-12
Table 1-3: Attenuator control settings.....	1-13
Table 1-4: Frequency band selection.....	1-16
Table 1-5: Attenuator selection.....	1-18
Table 1-6: Interrupts and chip selects	1-30
Table 1-7: Memory bank addressing.....	1-30
Table 1-8: Interrupt lines	1-32
Table 1-9: Latch control lines	1-33
Table 1-10: Buffered chip selects.....	1-33
Table 1-11: Power supplies.....	1-39

Introduction

The 2023 and 2024 AM/FM Signal Generators cover the frequency ranges 9 kHz to 1.2 GHz (2023) and 9 kHz to 2.4 GHz (2024). Output levels from -137 dBm to +13 dBm are available. A factory fitted option is available to extend the level to +25 dBm (+19 dBm above 1.2 GHz). Fig. 1-1 is a block diagram of the frequency synthesis and signal processing circuits.

Synthesiser

A VCXO operating at 100 MHz is phase locked to the internal (or external) frequency standard using a phase comparator at 10 MHz. The VCXO signal is divided by 20 to give a 5 MHz reference frequency for the fractional-N loop phase comparator.

A fractional-N loop is used to lock a multiplied low noise VCO to the reference with a resolution of 1 Hz. The VCO tunes from 400 to 533 MHz and is multiplied by 3, 4 or 5 to yield a signal in the range 1.2 to 2.4 GHz. A high speed programmable divider is used to divide the multiplied VCO frequency down to 5 MHz and a phase comparator compares this signal with the reference derived from the VCXO. The output from the phase comparator corrects the VCO frequency. In order to provide the required division ratio, the programmable divider is required to act as a fractional divider. The fractional-N gate array controls the division ratio of the programmable divider. The variation of this division ratio by the controller enables the loop to lock, with non-integer division ratios, to the reference with the resolution of 1 Hz without introducing spurious signals.

FM is produced using a two point modulation scheme. The FM signal is inserted into the loop by summing the FM signal with the VCO tune line to modulate the VCO directly. Simultaneously, the FM signal is fed to the fractional-N controller via a 1-bit oversampled A-D converter which converts an analogue input into a bit stream of '1's and '0's. The controller uses this input to modulate the division ratio in sympathy with the modulation. This allows frequencies less than the loop bandwidth, including DC, to modulate the output frequency.

In order to maintain good FM performance of the two point modulation system, the VCO FM tracking characteristics are required to be known. The sensitivity of the FM system via the 1-bit oversampled A-D converter is VCO independent and accurately calibrated by a DC calibration system. The VCO tracking is derived by an automatic FM SELFCAL routine during calibration. During an FM SELFCAL, the error signal on the tune line, for a frequency near the loop bandwidth, is monitored while varying the FM calibration numbers, allowing the variation in VCO sensitivities to be calibrated out. This will remove any perturbation of FM flatness near the loop bandwidth due to mismatch of two modulation paths.

RF processing

The VCO on board AA1 operates in the range 400 to 535 MHz and feeds to a harmonic generator whose 3rd, 4th and 5th harmonics are selected by voltage tuned band-pass filters to provide a frequency in the range 1.2 to 2.4 GHz. To generate frequencies below 1.2 GHz this signal is divided by factors of 2 to produce frequencies in the range 10 MHz to 1.2 GHz. A bank of switched half octave harmonic filters follows which is used to reduce unwanted harmonics at the output. Then the signal passes through the amplitude modulator where the output level envelope is controlled. The output from the modulator is peak detected. For frequencies less than 10 MHz the signal is mixed with an input from the 100 MHz VCXO. The resulting output in the frequency range 9 kHz to 2.4 GHz is fed from the output amplifier to attenuator board AA2. For pulse operation the signal is taken to the pulse modulator which operates in the range 30 MHz to 2.4 GHz. Otherwise the pulse modulator is bypassed and the signal is fed to the output attenuator. This is controlled by relays and provides attenuation in steps of 11 dB up to 132 dB. The attenuator also includes an RPP (Reverse Power Protection) system to protect the instrument from accidental application of reverse power.

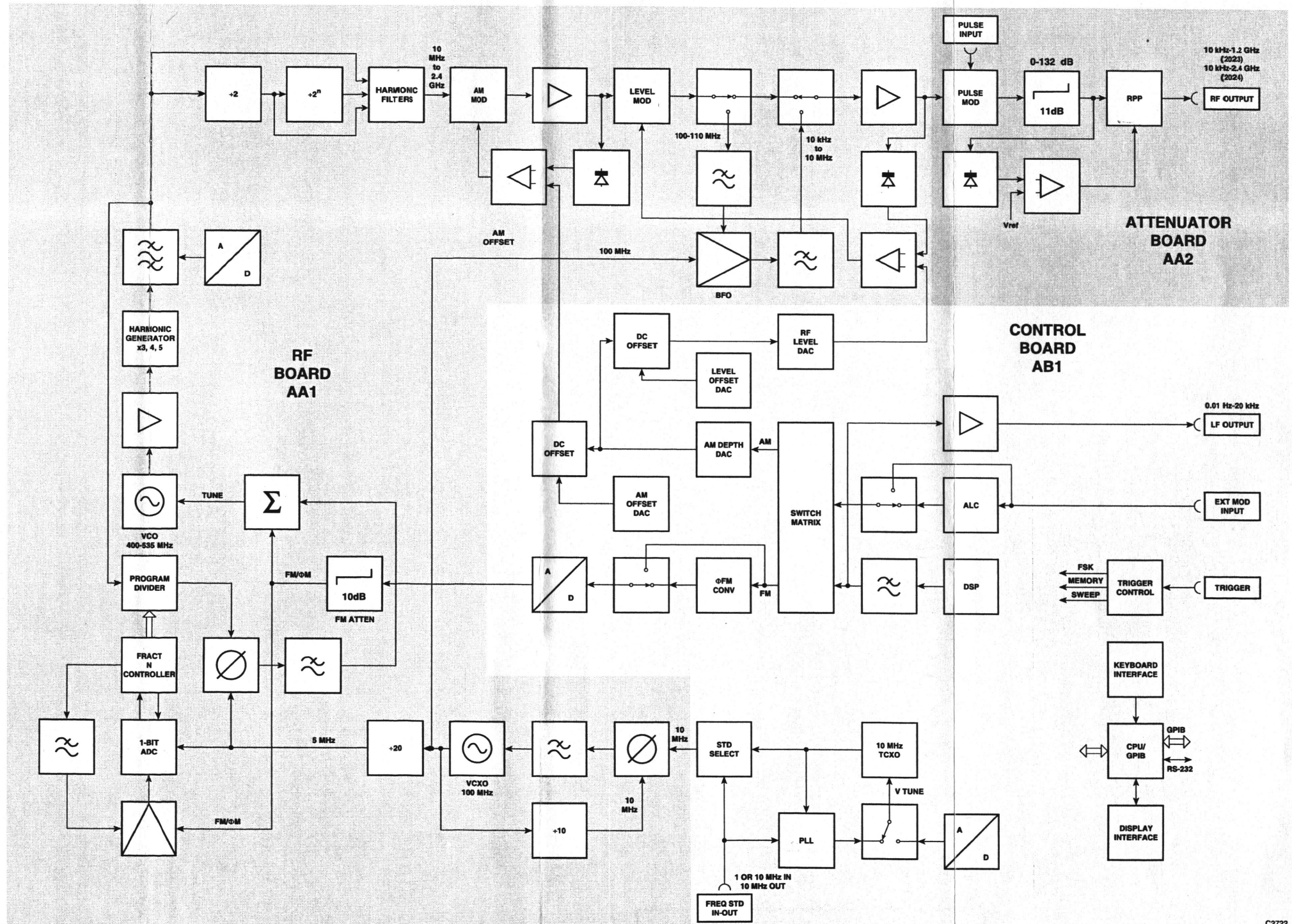


Fig. 1-1 Signal generator block schematic

C2722

Signal generator block schematic

LF processing

The LF processing all takes place on control board AB1, and may be conveniently subdivided into the following major functional elements.

LF output

A DSP (Digital Signal Processor) is used to generate the audio frequency signals used for internal modulation. One output from the DSP is used to supply the front panel LF OUTPUT socket.

For external modulation the signal applied to the EXT MOD INPUT socket first passes through AC/DC coupling selection and then can either be applied directly or via an ALC (Automatic Level Control) circuit to the audio multiplexers. The external direct signal can also be summed with the audio frequency from the DSP.

AM and level control

For amplitude modulation the modulation depth is set by a 12-bit A-D converter. A second A-D converter is used to produce the ALC reference for the RF board. Square law correction is applied to both signals.

FM/ ϕ M

For frequency modulation the signal amplitude controls the FM deviation. For phase modulation the signal is passed through a differentiator circuit.

RF board - AA1

Servicing diagrams: Figs. 7-2 to 7-22.

Carrier frequency synthesis

The RF carrier of the instrument should be as clean in frequency (and level) as possible. To achieve this goal the instrument relies on a single loop fractional-N Synthesiser scheme and a harmonic multiplier and UHF oscillator covering the fundamental range from 1.2 to 2.4 GHz. Using this approach minimises the RF processing circuitry normally associated with conventional frequency doubling or mixing schemes.

A carrier frequency resolution of 1 Hz cannot be achieved easily without the use of non-integer division. In this instrument this operation is controlled by a dedicated ASIC which modifies the division ratio of a programmable divider so that the average frequency is a non-integer division of the input.

RF board: Carrier generation (AA1 sheet 1)

Circuit diagram: Fig. 7-5.

Frequencies from 1.2 to 2.4 GHz are generated by multiplication from a 400 to 535 MHz low-noise oscillator. The tuned circuit is formed by C102, C108, varactor diodes D101 to D106 and printed inductors. A maintaining transistor TR101 is tapped into the tuned circuit. The oscillator is tuned by a differential voltage applied to the varactor diodes via L101 to L103. The VCO TUNE LOW line is used to phase lock the oscillator and inject FM whilst the VCO TUNE HIGH line is used to pre-steer the VCO.

The signal from the VCO is buffered by IC101 and then amplified by TR102 to provide a suitable level to drive the harmonic multiplier. The collector of TR102 is tuned by L104, C114 and C116. Harmonics are generated by D107 which acts as a step recovery diode. The diode is self-biased to improve the efficiency of harmonic generation by the network R110, R108 and C111. The harmonics generated by D107 are filtered by a four stage band-pass filter with a centre frequency in the range of 1.2 to 2.4 GHz. Each filter stage is formed by a pair of parallel coupled lines. Each line is capacitively loaded at one end by a pair of back to back varactor diodes to allow tuning over an octave. The stages are separated by buffer amplifiers IC104 to IC107. These amplifiers compensate for the loss and frequency response inherent in each filter stage and provide isolation so that tuning of the stages is independent. A pad at the output of each buffer amplifier increases the isolation and provides a better match to the input of the next filter stage. The filtered signal at the output of IC107 is split by R149 and R150 to feed the Synthesiser dividers (sheet 3) and the output dividers (sheet 7). The filter stages are tuned by a voltage in the range of 1 to 20 V derived from octal DAC IC103. This is applied via scaling amplifier IC102a and buffer IC102b. Diodes D125 and D126 allow fast tuning by shorting out R124 to reduce the charging time constant and so shorten the filter settling time whenever the frequency is changed. A 1.25 V reference for the DAC is provided by IC108 via IC102c. Table 1-3 below gives the relationship between the VCO frequency, the harmonic and the final output frequency.

Note

When the varactor diodes (D108 - D123) need replacing, then they must be replaced as a set. If the alternative type diodes are fitted resistor R717 will need repositioning accordingly.

Table 1-1: Carrier generation

Output frequency (MHz)	Harmonic number (N)	VCO frequency (MHz)
1200 - 1600	3	400 - 533.3
1600 - 2000	4	400 - 500
2000 - 2400	5	400 - 480

RF board: VCXO loop (AA1 sheet 2)

Circuit diagram: Fig. 7-7.

100 MHz VCXO

The 100 MHz VCXO is used to derive all of the clock signals necessary for the fractional-N Synthesiser. The use of a high frequency eliminates the need for a second phase locked oscillator to generate the necessary local oscillator frequency for the BFO. The reference divider provides a 5 MHz clock for the fractional-N Synthesiser and the FM A-D converter.

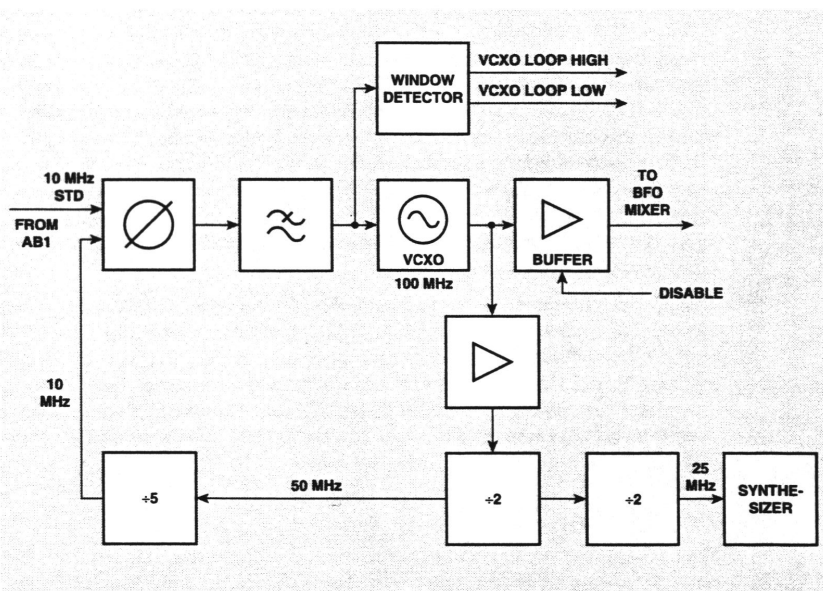
VCXO operation

The 100 MHz oscillator is built around TR201. Crystal XL201 together with L202 and D201 provide a series resonant circuit in the emitter circuit of TR201. At resonance it increases the gain of the common emitter stage and together with 180 degree phase shift network L204, C216, C215, C219 and C220 connected between the base and collector of TR201 provides the necessary conditions for oscillation. L203 tunes out the parasitic capacitance of the crystal package and prevents other spurious oscillations from occurring.

A facility to fine tune the phase shift network is provided by C215. At the resonant frequency the circuit operates at maximum power levels when the correct phase shift is achieved around the transistor. TR202 provides a buffered signal to the VCXO loop divider IC205. A second buffer, TR203 provides local oscillator drive (at typically +3 dBm) to the BFO mixer (sheet 9). The BFO DRIVE line to TR204 allows the second buffer amplifier to be powered down when the BFO is not in use to prevent leakage of the 100 MHz LO onto the instrument output.

100 MHz phase locked loop

The VCXO is used to provide a reference signal to the fractional-N loop and to the BFO band mixer and is locked to the 10 MHz frequency standard provided from control board AB1 via PLAB. The buffered 100 MHz signal is divided down to 10 MHz before phase comparison. An integrator and active low-pass filter ensures the removal of the reference frequency from the VCXO tune line. A window comparator monitors the VCXO tune line to detect when the oscillator is outside its normal operating range. The block diagram of the phase locked loop is shown in Fig. 1-2.



C2737

Fig. 1-2 100 MHz phase locked loop

Loop operation

The 100 MHz signal from the VCXO is buffered and amplified by TR205 to yield a CMOS logic compatible signal for the dividers which follow. The signal is divided by two by IC205a and then by five by IC202 to give 10 MHz for phase comparison. IC201 and IC203 form the loop phase frequency comparator. R203 and C208 remove the fast edges from the output of the phase detector. A broken integrator is formed around IC204b. This has a break frequency of 80 Hz and a gain at high frequency of four. IC204a, which follows, is a second order active low-pass filter with a cut-off of 700 Hz and a gain of two. The resulting loop bandwidth is approximately 150 Hz. The output from the active low-pass filter is further filtered by R212 and C213 to remove any high frequency signals.

IC204c and d form a window comparator which detects when the VCXO tuning voltage range is exceeded. The outputs from the comparators are attenuated to logic levels by R216 to R219 to give VCXO LOOP HIGH and VCXO LOOP LOW lines to provide status interrupts to the main processor via IC704 (sheet 8).

RF board: Synthesiser (AA1 sheet 3)

Circuit diagrams: Fig. 7-9.

Synthesiser operation

Frequency synthesis control is performed by a dedicated ASIC, IC305. This generates all of the necessary division ratios for programmable divider IC307 to synthesise any frequency within the range 1.2 to 2.4 GHz. Synthesiser operation is summarised in Fig. 1-3.

The 1.2 to 2.4 GHz input signal from the harmonic generator (sheet 1) is buffered by TR305 (sheet 3) to prevent divider spurious signals from IC309 reaching the instrument output. Signal feedback is not used with this stage to give high reverse isolation.

The buffered signal is divided by two by IC309 and then amplified by IC308 to obtain a sufficient level to drive the input of programmable divider IC307. The programmable divider is used to provide integer division in the range 120 to 240. Fractional division is achieved by the modification of the integer division ratios, under the control of ASIC IC305, in such a way that the average frequency over time is not an integer division ratio of the original. Control inputs to IC307 are TTL compatible. The control outputs from ASIC IC305 are inverted by IC306 to provide the correct polarity for IC307. Resistors R316 to R323 and R343 to R350 reduce the amplitude of the control signals to 2.5 V. The outputs of IC307 are converted from ECL to TTL levels by differential pair TR302 and TR303 and a single-ended amplifier TR304. Diode D307 provides schottky clamping for TR304 to ensure fast switching. The signal on the collector of TR304 is an all active edge squarewave at a 2.5 MHz rate. The fractional control ASIC and phase detector both require a clock with active positive edges. IC310d converts the 2.5 MHz signal to a 5 MHz signal with a short duty cycle and an active positive edge. The remaining gates of IC310 provide buffering. The division ratio generated by ASIC IC305 will be modified every time a positive edge is received at pin 51.

The reference for the main loop is obtained by dividing the 25 MHz signal present at IC302 pin 2 by five. The output of IC302 pin 11 is a 5 MHz rate pulse with a duty cycle of 40 ns. The clock for the 1-bit oversampled A-D converter is obtained from IC302 pin 13 after buffering and inversion by IC303a. The reference and divided output signal are compared by a phase frequency comparator comprising IC311, IC312b and IC313a. The phase detector output to the loop integrator and filter is available on pin 12 of IC311d. Under normal phase lock this will be a 5 MHz squarewave with nearly 50% duty cycle.

1-bit A-D converter

The DC input path to the Synthesiser consists of a third order, single bit, oversampling A-D converter, whose bit stream output is used to dynamically control the Synthesiser frequency via the Synthesiser ASIC.

Pin 6 of IC301b is used as the summing junction for four currents. These are: the input current from control board AB1 via R307 and R352; a negative offset current via R306; the bit stream feedback via R310; and the DC nulling offset current via R311. IC301b integrates the sum of these currents, and its output is further integrated by broken integrators IC301c and d. In these, when the frequency rises to a point where C301 and C302 are at low impedance, the ICs act as unity-gain amplifiers. Diodes D301 to D304 are used to enable the converter to recover cleanly from an overload.

The output from the last integrator is fed via comparator TR301, which converts the input to TTL levels, to D-latch IC304a, which is clocked at the same rate as the Synthesiser ASIC. The output from the D-latch is fed back into the summing junction to close the converter control loop. The output from IC304a is a pseudo random bit stream that represents the analogue FM input to IC301b. The bit stream is used by the Synthesiser ASIC to control the main carrier frequency.

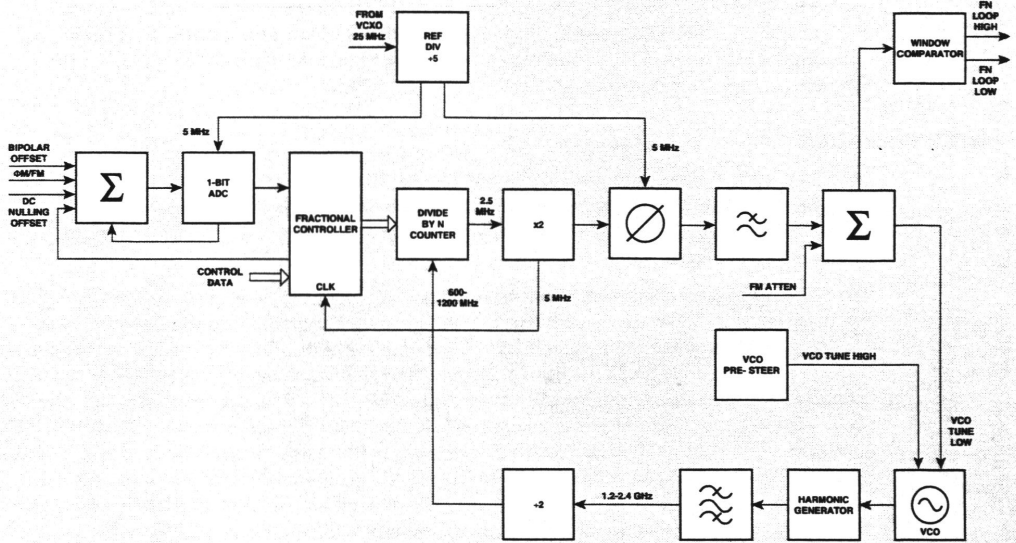


Fig. 1-3 Frequency synthesis

The DC nulling offset current is supplied from a 1-bit oversampling D-A converter in the Synthesiser ASIC. This balances the input current to make the converter read zero when DC nulling and when in AC coupled FM mode.

RF board: Loop filter and autocal (AA1 sheet 4)

Circuit diagrams: Fig. 7-11.

Loop filter

The input on the PHASE DETECTOR line is filtered by R404 and C401 to remove fast edges before the signal reaches loop integrator IC402. The loop integrator has a break frequency set by C402 of approximately 1.5 kHz and gain at high frequency of 1.2. The network R414, R415, C405 and C406 provides rejection of unwanted noise in the 10 to 30 kHz range without introducing a large phase shift at the loop bandwidth. IC404 is a unity gain second order active low-pass filter with a cut-off frequency of 40 kHz. The filtered signal from IC404 is attenuated

and summed with the FM drive signal on the FM ATTEN line by R433. This results in the VCO TUNE LOW output to the VCO (sheet 1). Loop bandwidth is approximately 3 kHz.

Correct phase lock is monitored by IC406c and d which detect when the voltage at the output of IC406a exceeds ± 8 V. Hysteresis is provided by R443 and R444. The detected outputs from D408 and D409 on the FN LOOP HIGH and FN LOOP LOW lines are attenuated to logic levels by R449 to R452. Loss of phase lock is signalled by interrupting the main processor via IC703 and IC704 (sheet 8).

VCO pre-steer

The VCO PRE-STEER voltage is generated by octal DAC IC103 (sheet 1). The signal from the DAC is amplified by IC401a and b to provide a tuning voltage in the range 1 to 22 V. Temperature compensation for the VCO is provided by D414. The network comprising TR403 to TR405 allows the pre-steer voltage to swing to within 0.5 V of the positive rail. Under normal operation the pre-steer voltage is filtered by R423 and C411 to prevent noise injection onto the VCO tune line. Diode D415 and IC408 allow fast tuning by shorting out R423 to reduce the charging time constant. IC408 is only switched on using the PRE-STEER SWITCH line during frequency changes that involve updating the pre-steer voltage.

Autocalibration

Dedicated hardware has been added to the Synthesiser to allow fast automatic calibration of the VCO pre-steer and FM frequency response. Pre-steer calibration is achieved by minimising the loop error voltage present at the output of IC406a. This is achieved by IC406b which forms a simple zero-crossing detector.

The FM frequency response calibration is performed by applying FM to the carrier with a 2 kHz modulating tone. Calibration is performed by minimising the amplitude of the resulting 2 kHz tone present at the output of the loop filter. The magnitude of the FM drive voltage applied to the VCO is adjusted automatically whilst the phase relationship between the loop error tone and the applied modulating tone is monitored. The correct drive level is found at the point where the phase switches from being in phase to being out of phase. IC407a is used to amplify the loop error tone. TR402 and C417 are used to implement a crude charge pump phase detector. IC407d is used to clip the 2 kHz modulating tone so that TR402 gate is driven with a squarewave. The output from the phase detector is filtered by two RC sections and buffered by IC407b. The sign of the filtered voltage, and hence the point of phase reversal is monitored by IC407c. The output of IC407c is converted to logic levels by D412, R457 and R458. Forward biasing D404, D405, D411 and D413 using the CAL DISABLE line suppresses the operation of the autocalibration hardware.

AA2 board identification

The AA2 BOARD SENSE line indicates one of three conditions to the processor: a standard attenuator board AA2 is fitted; a high-power attenuator board AA2/1 is fitted ; no attenuator is fitted. PLAE 15 indicates these conditions respectively by being: shorted to earth; open circuit; connected to earth via a 1 k Ω resistor. The two output lines BOARD ID (A) and BOARD ID (B) are connected by pull-up resistors R723 and R724 to IC705 (sheet 8). The logic is shown in Table 1-2. below.

Table 1-2: Attenuator board identification

PLAE 15	TR406	TR407	BOARD ID	
			(A)	(B)
Shorted to earth	OFF	OFF	H	H
Open circuit	ON	ON	L	L
Resistor	ON	OFF	L	H

Power amp cal comparator

Comparator IC401c compares the power amplifier detector level output from high power attenuator board AA2/1 with the POWER AMP CAL signal on IC401c pin 10. The latter signal comes from DAC IC103 (sheet 1). The comparator circuit performs a dual function. In instrument calibration mode the AA2/1 detector output is calibrated using the POWER AMP CAL signal to find the 'trip level' i.e. when the POWER AMP CAL output changes state. In normal instrument operation the high power DAC signal is set 6 dB below the expected detector level. Then, if due to some failure the power amplifier output falls by more than 6 dB, POWER AMP CAL will flag an error, resulting in an error message being generated on the screen.

RF board: FM drive (AA1 sheet 5)

Circuit diagram: Fig. 7-13.

FM adjusts the instantaneous RF frequency in direct sympathy with the modulating signal. The amount of frequency deviation is directly proportional to the magnitude of the modulation source. With phase modulation the frequency deviation is also proportional to the frequency of modulation.

For moderate modulation rates the signal is injected straight onto the VCO tune line after suitable scaling by D-A converters (giving fine control) and fixed attenuators (giving coarse control). The block diagram of the FM drive is shown in Fig. 1-4.

Inside the loop bandwidth this method is not valid as the loop cannot distinguish between FM and other VCO frequency errors. It would therefore try to compensate for the modulation tone by returning the carrier back to the original requested frequency. A digital system is used to overcome this effect, which also has the benefit of extending the modulation range down to DC.

The modulation is sampled by a 1-bit oversampling A-D converter whose output controls the Synthesiser gate array controller ASIC in such a way as to offset the carrier frequency in proportion to the magnitude of the modulation. The speed at which the ASIC can perform this function sets a limit to the overall bandwidth of the system. At frequencies above the loop bandwidth the analogue system dominates.

Operation

The FM input to the RF module feeds the 1-bit oversampling A-D converter and the analogue FM attenuator. The analogue attenuator provides the FM drive signal to the VCO and consists of 2 stages. A 12-bit multiplying D-A converter IC409, allows fine setting of the FM drive level. Coarse setting is achieved by IC403 and by a pad switched by RLA. IC403 is an analogue multiplexer and is used provide attenuation of 0, 20 or 40 dB and can be used to connect the FM input to ground. IC405a has 10 dB of gain and provides a high current drive for the final attenuator stage. The final attenuator stage is switched by RLA and gives either 10 or 50 dB of attenuation. The output from the final attenuator stage on the FM ATTEN line is summed with the control voltage from the fractional-N loop across R431 and R432 (sheet 4) which provides a 25 Ω drive to the VCO. The FM attenuator control settings are given in Table 1-3.

Table 1-3: Attenuator control settings

Atten (dB)	AT2	AT1	AT0
OFF	0	0	0
20	1	0	0
40	1	1	0
60	0	1	0
80	0	1	1

VCO FM tracking autocalibration is performed by IC407 and associated circuitry (see 'Autocalibration' above for details). Digital FM and FM at low modulation frequencies is

achieved by the combination of the 1-bit oversampled A-D converter formed by IC301, IC304a and Synthesiser ASIC IC305 (sheet 3). The A-D converter samples the modulation source at a high rate and passes the information to the gate array controller in a high speed serial data stream. The ASIC then modifies the control to the main divider IC307 to change the instantaneous frequency of the carrier.

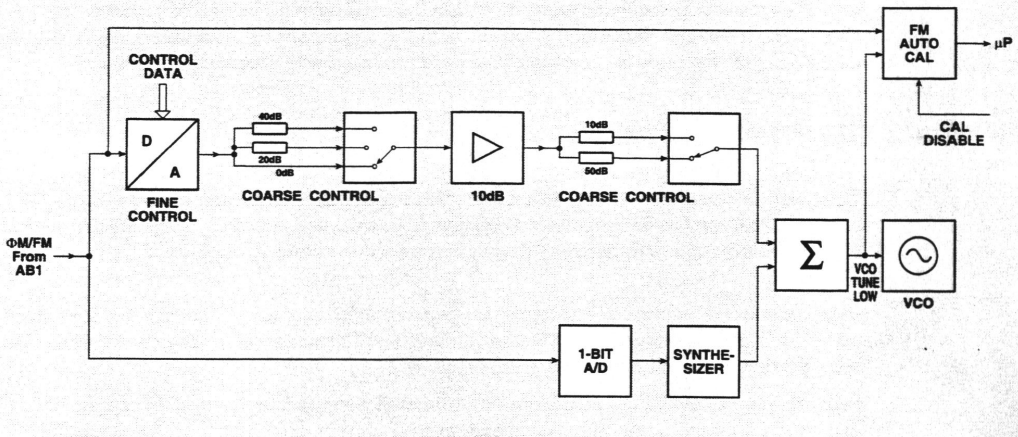


Fig. 1-4 FM/φM drive

RF board: Level modulator (AA1 sheet 6)

Circuit diagram: Fig. 7-15.

Amplitude modulator

The amplitude modulator is responsible for applying amplitude modulation to the carrier. To do this a voltage-controlled pin diode modulator and envelope detector are used in a control loop to apply amplitude modulation to the RF carrier. The control voltage from the control board is predistorted before it is applied to the control loop to compensate for the inherent non-linearity of the Schottky diode detector used for envelope detection.

PIN modulator

Diodes D501 to D507 are the pin diodes arranged as a dual Π modulator. Transistors TR501 and TR502 form a pair of voltage controlled current sinks which produce complementary output currents, one to drive the series diodes and one to drive the shunt diodes. Resistor R513 sets the transconductance of these current sinks and hence the gain of the pin modulator. Capacitor C523 across R513 helps to speed up the modulator by providing lead compensation for the pin diodes; the time constant of R513 and C523 being approximately equal to the charge lifetime of the pin diodes. Resistors R509 and R511 are required to source current into the diodes when stored charge needs to be removed quickly from the diodes since internal recombination alone is far too slow.

Transistors TR506 and TR510 are two similar RF amplifying stages. TR506 recovers losses from the pin modulator and TR510 recovers losses from the divider and filter stages (sheet 7). Since the same DC biasing is used for both stages only one stage, that for TR506, will be described. Resistors R516 and R542 fix the base voltage on TR503 which in turn sets the collector voltage on TR506. The collector current is set by the value of R524. A two-inductor combination, L505 and L506, is used to isolate the RF line from the DC circuitry. Diode D515 compensates for the

TR503 base-emitter variations with temperature. Resistors R521, R546, R547 and R555, R556 set the RF gain of this stage.

The control voltage input to the modulator is converted into a digital word by an analogue to digital converter. This converter is implemented with comparator IC501a and FILTER CAL from one of the DACs in IC103, the status of the comparator being available as FILTER PEAK. This measurement is used for self-calibration of the voltage-tuned band-pass filters on sheet 1 and also for instrument fault diagnosis.

Peak detector and control loop

D510 is the Schottky detector diode used to detect the peak RF voltage on the microstrip line. The output from this detector is not linear at low RF levels but obeys a square law transfer function, hence if modulation distortion is to be eliminated, the control voltage from the control board must compensate for this effect. Schottky diode D511 is used for temperature compensation of D510. The modulation voltage on the AM INPUT line from control board AB1 is larger than that required by the control loop and is attenuated by R527 and R517. The voltage level from the control board is approximately 1.4 V average with the modulation superimposed on it. An error amplifier consisting of IC802a amplifies the differential error voltage between the modulation input and the detector output. The output of this error amplifier then controls the pin modulator as necessary to keep the error voltage as small as possible. Feedback in the form of C511 and R526 reduces the effective gain and phase shift of the error amplifier at high frequencies to ensure adequate gain and phase margins.

Level modulator

The level modulator is based around PIN diodes D512 and D513 and is split into two sections with amplifier stage TR508 in between. The input level to the modulator is nominally -4 dBm (10 MHz to 2.4 GHz), and it has an inherent loss of up to 3 dB. The modulator diodes are controlled by the LEVEL MOD input line from levelling loop integrator IC802 (sheet 9). The loop integrator input (in the range ± 10 V) sets the amount of current through diode packages D512 and D513 by controlling TR504 and TR505 collector current levels. When D512 and D513 pins 1 are at -10 V the two series diodes are fully ON and the shunt diode is reverse biased, resulting in minimum RF signal loss (low attenuation limit). When D512 and D513 pins 1 go positive with respect to pins 3 and 4, the two series diodes become reverse biased and the shunt diodes forward biased resulting in maximum RF signal loss in the modulator (high attenuation limit). TR507 sets the DC biasing condition for TR508.

Output unlevelled

The comparator configuration around IC501b detects the condition where the level modulator drive signal gets close to the positive supply rail value. It compares the LEVEL MOD input with the +11 V supply and signals on the OUTPUT UNLEVELLED line that the level modulator is close to or at the minimum attenuation limit and therefore the output may be unlevelled.

Pulse modulation drive

The pulse modulator driver is based around IC503a and is basically a level translating buffer stage. The input on the PULSE I/P line from control board AB1 to the driver is at TTL levels. The output is clamped by zener diodes D508 and D509 at approximately ± 8 V. When the input is LOW (0 V) the output is at -8 V and when the input is HIGH (+5 V) the output is at +8 V. The output on the PULSE O/P line drives the pulse modulator on attenuator board AA2. When the pulse signal input is LOW, the pulse modulator goes into low isolation (RF ON) mode and vice versa.

RF board: Frequency generator (AA1 sheet 7)

Circuit diagram: Fig. 7-17.

Frequency generation

A UHF VCO, step recovery diode and voltage tuned band-pass filter (sheet 1) are used to generate a fundamental octave between 1.2 and 2.4 GHz which is phase locked to the instrument reference.

To generate frequencies below 1.2 GHz, a fixed +2 prescaler and a programmable +2ⁿ prescaler (on this sheet) are used to divide the input frequency of 1.2 to 2.4 GHz down to frequencies between 10 MHz and 1.2 GHz. Switched low-pass filters (LPF) are then used to reduce unwanted harmonics at the output. To produce frequencies between 10 kHz and 10 MHz, the 100 MHz instrument reference is mixed with the divider generated signal of between 100 MHz and 110 MHz to produce a beat note below 10 MHz (sheet 9).

Frequency band selection

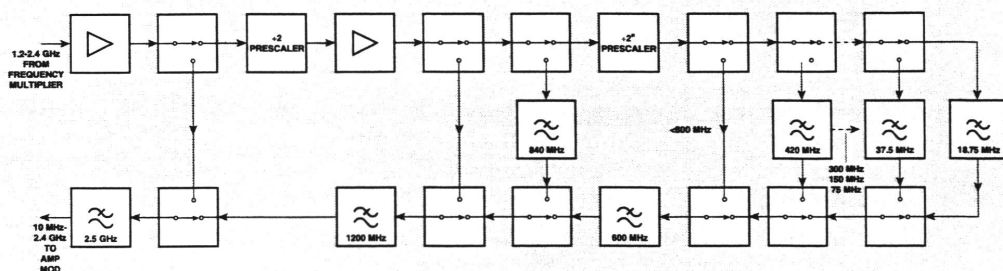
A serial communications link between the RF board and control board AB1 is used to control the operation of the RF board. Data latch IC709 (sheet 8) converts the serial data input from the control board into the parallel control bits required to select a particular frequency band. Frequency band selection is shown in Fig. 1-5.

Four control bits (BS0 to BS3) are required to specify the required frequency from the dividers and filters. Control bit BS0 selects the upper or lower 1/2 octave but is only required for selected frequencies between 300 MHz and 1.2 GHz and is set to zero for selected frequencies outside these limits (BS0 is set high for the lower 1/2 octave). Control bits BS1 to BS3 select the required octave of output frequency from the dividers. Table 1-4 below lists the control bits required for the selection of each frequency band.

Table 1-4: Frequency band selection

BS3	BS2	BS1	BS0	Selected band
0	0	0	0	420 - 600 MHz
0	0	0	1	300 - 420 MHz
0	0	1	0	150 - 300 MHz
0	1	0	0	75 - 150 MHz
0	1	1	0	37.5 - 75 MHz
1	0	0	0	18.75 - 37.5 MHz
1	0	1	0	10 - 18.75 MHz
1	1	0	0	1.2 - 2.4 GHz
1	1	1	0	0.84 - 1.2 GHz
1	1	1	1	600 - 840 MHz

This particular mapping enables these same control bits to be used for LPF selection as well as to control the division ratio of IC602 which is a programmable divider. IC603 and IC608 are each three to eight line decoders which produce a logic low level on the particular output specified by the band selection bits, all other outputs remaining high. Each of the decoder outputs corresponds to one particular signal path which is switched in with pin diodes. These pin diodes cannot operate directly with standard logic levels so IC604 to IC606 convert the logic level outputs of IC603 and IC608 into the required levels for driving the pin diodes.



C2735

Fig. 1-5 Frequency band selection

Fundamental octave

The 1.2 to 2.4 GHz from the voltage tuned band-pass filter (sheet 1) is the fundamental octave and is amplified by IC607 to ensure adequate drive for the subsequent circuitry. When a frequency within this fundamental octave is selected, the 1.2 to 2.4 GHz switch is selected by the SW1 control line going negative. Diodes D603 to D605 are then reverse biased whilst a half each of diodes D601 and D602 are forward biased. Hence the prescalers and sub 1.2 GHz filters are bypassed. The printed 2.5 GHz LPF at the output is permanently in circuit to remove harmonics and spurious signals above 2.5 GHz.

600 MHz to 1.2 GHz generation

IC601 is a fixed +2 prescaler used to divide the fundamental octave down to between 600 MHz and 1.2 GHz. TR606 and R636 are used to bias IC601 off when not required, this prevents IC601 from self-oscillating. TR601 is selected whenever one of switch lines SW2 to SW10 is low, TR601 being used to detect this condition, switch TR606 off as required and hence enable IC601. The output level of this prescaler is not high enough to drive programmable prescaler IC602 directly, so TR603 and TR604 form a balanced amplifier to boost the output level. When 600 MHz to 1.2 GHz is selected, balun T601 transforms the amplified balanced output of IC601 into an unbalanced output appropriate for microstrip, D607 being used to connect one output of T601 to ground.

The 600 MHz to 1.2 GHz octave is split into two half-octaves because the second harmonic content of the output is too high to allow octave filtering.

The 1200 MHz LPF is permanently in place for frequencies below 1.2 GHz and a simple switch consisting of D608 to D612 is used to route the output of T601 through to the 1200 MHz filter. The sub 840 MHz half-octave path switch is similar but also contains the 840 MHz LPF.

Programmable divider

IC602 is the programmable divider which is used to produce frequencies down to 10 MHz. This divider is only useable up to 1.5 GHz, hence the need for prescaler IC601 which is useable to at least 2.5 GHz. The required division ratio is set by control bits BS1 to BS3 and represents a power of 2. The division ratio selected is related to the selection bits by the following expression:

$$\text{Division ratio} = 2^{((4 \times \text{BS3}) + (2 \times \text{BS2}) + \text{BS1} + 1)}$$

The output of IC602 is balanced and is converted to a single ended output by balun T602 which is identical to T601. The output level of this divider is already high enough not to require any extra amplification. For frequencies below 300 MHz, the output is balanced well enough to require

only octave filtering thereby reducing the number of filters required to meet the harmonic performance requirement. Between 300 MHz and 600 MHz however, two half octave filters are used. D606 and R635 are required to short out the 600 MHz LPF when the 840 MHz filter is selected to prevent D615 from resonating with the 600 MHz filter.

RF board: Interface and attenuator drive (AA1 sheet 8)

Circuit diagram: Fig. 7-19.

Serial bus interface

The serial bus from control board AB1 is connected to PLAC and fed to serial to parallel converters IC702 and IC706. These ICs supply address and data information to the fractional-N controller (sheet 3) and data to decoder IC707. The outputs from IC707 provide clock signals to parallel to serial converters IC708 to IC710 and enable signals to IC704 and IC705. AT0 to AT2 from IC708 select the FM drive fine setting. IC709 provides parallel control bits BS0 to BS3 used for frequency band selection.

IC704 and IC705 perform parallel to serial conversion for the transmission of board status signals to the processor. IC705 is monitored by the processor, and when OR-gate IC703 detects a fault condition e.g. RPP TRIPPED going high, the processor is aware of a fault condition but doesn't know what the fault is. It then performs a serial poll of the inputs to IC704 to determine the actual fault.

Attenuator drive

The attenuator pad data comes via the serial bus and is latched by serial-to-parallel converter latch register IC710. When a pad control line output is LOW (0 V) the corresponding attenuator pad is selected via one of the transistor switches TR701 to TR707. Conversely when the latch output goes HIGH (+5 V) the pad is deselected. There are five attenuator pads which need controlling, they are labelled PAD A (33 dB), PAD B (22 dB), PAD C (33 dB), PAD D (11 dB) and PAD E (33 dB). This gives a total attenuation of 132 dB, selectable in 11 dB steps. The pad control lines can source up to 200 mA. The pad selection combinations for any required attenuation setting are shown in Table 1-5 below.

Table 1-5: Attenuator selection

Attenuation	A (33 dB)	B (22 dB)	C (33 dB)	D (11 dB)	E (33 dB)
0	1	1	1	1	1
11	1	1	1	0	1
22	1	0	1	1	1
33	1	1	1	1	0
44	1	1	1	0	0
55	1	0	1	1	0
66	1	1	0	1	0
77	1	1	0	0	0
88	1	0	0	1	0
99	1	0	0	0	0
110	0	1	0	0	0
121	0	0	0	1	0
132	0	0	0	0	0

Pulse modulation

There are two control lines related to pulse modulation, one is the PULSE I/P line (sheet 6) which comes from the rear panel via control board AB1 and the other is the PULSE MOD ENABLE line obtained by decoding the serial bus. When the output is LOW the pulse modulator path is selected. Conversely when the output is HIGH the straight through path is selected and the pulse modulator is set to low isolation mode (pulse input set LOW). This line is capable of sourcing 200 mA.

RPP control

The Reverse Power Protection (RPP) circuit has two lines on this board. The RPP TRIPPED readback line from attenuator board AA2 is normally LOW and goes HIGH when the RPP has tripped. The RPP RESET control line is normally HIGH and switched LOW (for less than 1 ms) to reset the RPP relay.

High power amplifier option

The high power amplifier, when fitted, is switched on attenuator board AA2 by a single control line from this board. When the HIGH POWER ENABLE control line is LOW the amplifier is selected and when HIGH it is deselected.

RF board: output amplifier (AA1 sheet 9)

Circuit diagram: Fig. 7-21.

Output amplifier

The output amplifier consists of four, common emitter, transistor stages (TR806 to TR808 and TR814). The first two stages are only used down to 10 MHz and are switched OFF to obtain high isolation below 10 MHz. Frequencies between 10 kHz to 10 MHz are obtained by mixing the input with a 100 MHz local oscillator. The switching between these two paths from the MODULATED RF input is controlled by the BFO SELECT line. When this line is in LOW state, TR810 is OFF and TR811 is ON and the corresponding transistors TR801 to TR803 are ON and TR804 and TR805 are OFF. In this state transistors TR801 and TR802 set the RF transistors TR806 and TR807 in amplifying mode and TR805 sets TR812 in isolation mode. Transistors TR803 and TR804 set D801 bias by forward biasing the diode between pins 1 and 4 and reverse biasing the diode between pins 1 and 3, thereby selecting the high frequency path via C806. Conversely, when the BFO SELECT line goes HIGH, the high frequency path is set to isolation mode and the BFO low frequency path via C802 is selected. Since all four transistor amplifier stages have similar active biasing arrangements, only the final stage will be described here. Resistors R847 and R848 and diode D808 fix the base of TR809. TR809 in turn forward biases TR808 base-emitter junction until TR809 collector is one diode drop above the base potential. L808 has about 15 Ω winding resistance, and with R849 and R875 also set to 15 Ω , the TR808 collector current is approximately 110 mA with 16 V across it. Note that diode D808 is only added to temperature compensate the base-emitter junction voltage. Below 10 MHz the BFO path is selected and TR806 and TR807 are switched OFF; this results in D802 being reverse biased through R839. This increases the isolation of the straight through path.

Note

The lead dimensions of leaded capacitor and resistor components are critical to the instrument performance. Make sure these components are replaced in identical fashion.

BFO-band frequency generation

Transistors TR815 to TR820 are configured as a double balanced Gilbert cell mixer. The resistors improve the noise performance because the transconductance of the upper switching transistors is now limited by the resistors instead of increasing with the bias current. Hence the signal handling capability of the mixer can be improved, by increasing the bias current, without increasing the output noise. The disadvantage with this is that the local oscillator (LO) signal must now be larger to overcome the increased voltage drop across these resistors.

An LO level of 0.5 V is adequate to guarantee complete switching of the balanced signal currents from TR819 and TR820. The LO signal is derived from the 100 MHz internal reference on sheet 2, hence the input RF frequency to the mixer should be 100 MHz more than the desired output frequency. The RF input signal for the mixer is produced by the dividers and harmonic filters on sheet 6 and is switched into the mixer by D801 as described above. Output is on the RF OUTPUT line to attenuator board AA2.

RF levelling detector

The levelling detector is basically a directional bridge configuration based on D804. The detector has a good match at both ports but is relatively more sensitive to RF signals coming from output amplifier TR808 than to any signals travelling in the opposite direction. The main disadvantage with this arrangement is that the detector diode 'sees' only a fraction of the RF voltage. The detector diode is biased through R860 and R861 and the detected voltage appears on the INVERTING input of integrator amplifier IC802c. The input from 8-bit DAC IC103 (sheet 1) on the OFFSET TRIM line is used to calibrate out detector offsets. Diodes D805 and D810 are used to temperature compensate detector diode D804. The required RF level is set by applying twice the detector volts (of opposite sign) to the RF LEVEL input line from control board AB1.

ALC loop

The Automatic Level Control (ALC) requires an input voltage range of from 0 to -5 V with 12-bit resolution. The 0 V input corresponds to minimum RF level, and -5 V to the maximum level. The AM signal is superimposed on the level control voltage and the sum is prevented from exceeding the -5 V limit.

The 50 Hz low-pass filter based on IC802b in the level control loop, is used to limit the ALC bandwidth when the AM signal is applied. Normally, the filter is switched out of the loop as shown on the circuit diagram and the bandwidth is high, resulting in a short ALC settling time. When AM is selected the filter is switched in to stop the ALC loop removing the AM signal from the carrier. Capacitor C841 is also switched with the filter to keep the loop stable. Since the AM signal is also superimposed on the level control input, the AM is useable down to DC level.

The filter is switched IN and OUT of the ALC loop by IC803. The filter is selected when the AM-FILTER control line from IC709 (sheet 8) is HIGH and deselected when the line is LOW. The ALC output unlevelled status LEVEL MOD line is normally in a LOW state and goes HIGH when the modulator is driven hard on.

Offset trim

The +11 V supply line is monitored (sheet 9) to provide the OFFSET TRIM REF voltage for IC103 which, in turn, supplies the OFFSET TRIM output used to linearize the level detector.

RF board: Power supplies (AA1 sheet 10)

Circuit diagram: Fig. 7-22.

Power supplies

This sheet shows the board power supply lines together with the board power supply table. All unused IC sections are also shown.

Attenuator board - AA2

Servicing diagram: Figs. 7-23, 24.

Circuit functions

Circuit diagram: Fig. 7-24.

Attenuator board AA2 provides the following instrument functions:-

- (1) Pulse modulation facility.

- (2) Step attenuation in five switchable stages with a total attenuation depth of 132 dB.
- (3) Reverse Power Protection (RPP) facility.

Pulse modulation

The pulse modulator works from 30 MHz to 2.4 GHz with an ON/OFF ratio of greater than 40 dB. When the MOD line from RF board AA1 is LOW to RLA and RLB pulse modulation is selected; when HIGH the straight through path is selected. When the PULSE INPUT line is in the HIGH (+8 V) state series diodes D1 and D7 are reverse biased and the shunt diodes D2 to D6 are forward biased, shunting RF signal to ground. The shunt diodes are selected for very low ON resistance, which results in higher isolation. Resistors R1 and R2 are added to maintain reasonable input/output match to 50 Ω .

When the PULSE INPUT line switches to LOW (-8 V) state, the series diodes are forward biased and the shunt diodes become reverse biased, allowing RF signals to propagate from RLA to RLB with minimum attenuation. The shunt diodes are interconnected with thin inductive tracks such that, together with the diode capacitance, the circuit behaves like a low-pass filter with roll-off above the desired maximum frequency. This results in lower insertion loss and better matching characteristics.

C1, C2 and L1 as well as C3, C4 and L2 form high-pass filters. These filters attenuate the pulse modulating signals and thereby prevent their propagation down the RF lines. R3, L4 and L3 as well as R7, L8 and L7 form broadband RF chokes. Inductor L17 is inserted to arrest sharp pulse input rise/fall edges from the pulse drive circuit.

Attenuator

The attenuator section consists of five attenuating pads constructed from thick film resistors. There are three pads of 33 dB value and one each of 22 dB and 11 dB, giving a maximum attenuation depth of 132 dB. The four higher value pads consist of two Π resistor stages connected in series to facilitate the use of smaller value resistors, with lower parasitics, resulting in a flatter frequency response. These pads are switched with two separate relays in order to obtain greater isolation between the input and output of each pad. The 11 dB single relay pad is switched with a higher isolation type relay. All the relays are mounted on the ground side of the board and sit in individual 'pockets' in the RF module.

All relay control lines from RF board AA1 are decoupled using ceramic feedthrough Π filters. On some lines further decoupling is achieved by the addition of inductors L9 to L14 and capacitors C14 to C24. Diodes D10 to D15 are added to prevent damage to the relay drive circuitry on the RF board. Also two wall "intrusions" are introduced along the attenuator length to prevent surface wave propagation.

Reverse power protection

The Reverse Power Protection (RPP) consists of a reed-relay (RLM), capable of switching up to 50 W of RF power, with associated RF level detection and relay drive circuitry.

In normal operation the reed-relay contacts are closed and a small fraction of the RF voltage appears at the junction of R44 and R45. Both positive and negative RF voltage peaks are detected by the dual detector diode package D8. IC1 is a dual comparator package with open collector outputs. The peaks of the RF voltage waveform are detected by D8 and charge capacitors C8 and C9 to the peak RF level. When the voltage on C8, for a positive peak, becomes greater than the voltage threshold set on non-inverting input pin 3 of IC1a, the output of the comparator goes LOW switching TR1 OFF so that RLM becomes open circuit. In a similar fashion when C9 causes comparator IC1b non-inverting input pin 5 becomes more negative than inverting input pin 6, the output on pin 7 switches to the LOW state. The RPP trip status is indicated on the RPP TRIPPED line. High voltage zener diode D9 is used to limit the coil EMF voltage and to keep this voltage relatively high in order to quickly discharge the magnetic field and thereby shorten the relay switching time.

In normal operation TR1 is ON and the RPP RESET line is set HIGH keeping TR2 in the OFF state. When an overload occurs TR1 switches OFF as described above. This allows the collector voltage of TR1 to feed back to the inverting input of comparator IC1b inverting input, clamping it at a voltage greater than 0 V. This has the desired effect of preventing the RPP relay from being reset even after the RF signal has been removed. Thereafter the RPP can only be reset by switching the RPP RESET line LOW to switch on TR2, which, via IC1b, switches TR1 back into the ON state.

When an attenuator stage is switched between the two matched states, i.e. resistive pad or through line positions, the relay contacts momentarily become open circuit, creating a large standing wave. Inductors L15 and L16 are inserted to slow down these transients and thereby prevent false RPP trippers.

In order to keep board connections to a minimum, the +5 V line is generated locally using voltage regulator IC2.

High power attenuator board - AA2/1

Servicing diagrams: Figs. 7-25 to 7-27.

Circuit functions

Attenuator board AA2/1 provides the following instrument functions:-

- (1) Pulse modulation facility.
- (2) Step attenuation in five switchable stages with a total attenuation depth of 132 dB.
- (3) Switchable power amplifier stage with up to +25 dBm power output capability.
- (4) Reverse Power Protection (RPP) facility.

High power attenuator board: Pulse mod & attenuator (AA2/1 sheet 1)

Circuit diagram: Fig. 7-26.

Pulse modulation

The pulse modulator works from 30 MHz to 2.4 GHz with an ON/OFF ratio of greater than 40 dB. When the MOD line from RF board AA1 is LOW to RLA and RLB pulse modulation is selected; when high the straight through path is selected. When the PULSE INPUT line is in the HIGH (+8 V) state series diodes D1 and D7 are reverse biased and the shunt diodes D2 to D6 are forward biased, shunting RF signal to ground. The shunt diodes are selected for very low ON resistance, which results in higher isolation. Resistors R1 and R2 are added to maintain reasonable input/output match to 50 Ω .

When the PULSE INPUT line switches to LOW (-8 V) state, the series diodes are forward biased and the shunt diodes become reverse biased, allowing RF signals to propagate from RLA to RLB with minimum attenuation. The shunt diodes are interconnected with thin inductive tracks such that, together with the diode capacitance, the circuit behaves like a low-pass filter with roll-off above the desired maximum frequency. This results in lower insertion loss and better matching characteristics.

C1, C2 and L1 as well as C3, C4 and L2 form high-pass filters. These filters attenuate the pulse modulating signals and thereby prevent their propagation down the RF lines. R3, L4 and L3 as well as R7, L8 and L7 form broadband RF chokes. Inductor L25 is inserted to arrest sharp pulse input rise/fall edges from the pulse drive circuit.

Attenuator

The attenuator section consists of five attenuating pads constructed from thick film resistors. There are three pads of 33 dB value and one each of 22 dB and 11 dB, giving a maximum attenuation depth of 132 dB. The four higher value pads consist of two Π resistor stages

connected in series to facilitate the use of smaller value resistors, with lower parasitics, resulting in a flatter frequency response. These pads are switched with two separate relays in order to obtain greater isolation between the input and output of each pad. The 11 dB single relay pad is switched with a higher isolation type relay. All the relays are mounted on the ground side of the board and sit in individual 'pockets' in the RF module.

All relay control lines from RF board AA1 are decoupled using ceramic feedthrough Π filters. On some lines further decoupling is achieved by the addition of inductors L9 to L14 and capacitors C8 to C17 and C20. Diodes D8 to D13 are added to prevent damage to the relay drive circuitry on the RF board. Also two wall "intrusions" are introduced along the attenuator length to prevent surface wave propagation.

High power attenuator board: Power amp & RPP (AA2/1 sheet 2)

Circuit diagram: Fig. 7-27.

Power amplifier

The power amplifier consists of two RF amplifying stages and an RF detector for approximate level indication. The first amplification stage is based around transistor TR1. Feedback resistor R55 and the emitter resistors R47 to R50 set the low frequency gain of this stage; with the values shown the gain is approximately 12 dB. The inductor chain L15 to L17 and L24 forms a broad band RF choke. The biasing condition for this stage is controlled by TR3. The base of TR3 is fixed at approximately 17 V, this sets the R57/L24 junction around 17.7 V. Resistors R56 and R57 in turn set the collector current to approximately 100 mA. The gain of the amplifier drops with increasing temperature. This effect can be minimized by a gradual reduction in the collector current of TR1 with increasing temperature. Diodes D14 and D15 and the thermistor R51 are used to produce this desired effect. When the temperature increases, TR3 base potential rises resulting in a decrease in TR1 collector current. The current variation is only around $\pm 10\%$ over the 0 to 55°C temperature range. 3 dB attenuator pad R44 to 46 is inserted to improve the amplifier input match and thereby reduce the level inaccuracy due to mismatch.

The output RF transistor stage biasing configuration for TR2 is very similar to that for TR1. The collector voltage is fixed at around +16 V and the collector current is nearly 300 mA. Temperature compensation on this stage is very subtle in order to maintain high power output, with only a few milliamps of current variation available from diode pair D16 and D17.

Components R69 and C36 are inserted to selectively improve the low frequency output match. Diode detector D18 detects RF signals down to around +5 dBm. The difference between the detected voltage and the 'dummy' detector (D22) voltage is amplified by the difference amplifier based around IC02a. The dummy detector provides offset and temperature compensation.

Reverse power protection

The Reverse Power Protection (RPP) consists of a reed-relay (RLM), capable of switching up to 50 W of RF power, with associated RF level detection and relay drive circuitry.

In normal operation the reed-relay contacts are closed and a small fraction of the RF voltage appears at the junction of R72 and R73. Both positive and negative RF voltage peaks are detected by the dual detector diode package D19. IC1 is a dual comparator package with open collector outputs. The peaks of the RF voltage waveform are detected by D19 and charge capacitors C39, C40 and C41, C42 to the peak RF level. When the voltage on C39 C40, for a positive peak, becomes greater than the voltage threshold set on non-inverting input pin 3 of IC1a, the output of the comparator goes LOW switching TR6 OFF so that RLM becomes open circuit. In a similar fashion when C41, C42 causes comparator IC1b non-inverting input pin 5 becomes more negative than inverting input pin 6, the output on pin 7 switches to the LOW state. The RPP trip status is indicated on the RPP TRIPPED line. High voltage zener diode D20 is used to limit the coil EMF voltage and to keep this voltage relatively high in order to quickly discharge the magnetic field and thereby shorten the relay switching time.

In normal operation TR6 is ON and the RPP RESET line is set HIGH keeping TR9 in the OFF state. When an overload occurs TR6 switches OFF as described above. This allows the collector voltage of TR6 to feed back to the inverting input of comparator IC1b inverting input, clamping it at a voltage greater than 0 V. This has the desired effect of preventing the RPP relay from being reset even after the RF signal has been removed. Thereafter the RPP can only be reset by switching the RPP RESET line LOW to switch on TR9, which, via IC1b, switches TR6 back into the ON state.

When an attenuator stage is switched between the two matched states, i.e. resistive pad or through line positions, the relay contacts momentarily become open circuit, creating a large standing wave. Inductors L21 and L22 are inserted to slow down these transients and thereby prevent false RPP tripovers.

In order to keep board connections to a minimum, the +5 V line is generated locally using voltage regulator IC3.

Signal output board - AA2/2

Circuit diagram: Fig. 7-28.

Circuit function

This board is used when no attenuator is fitted, where it serves to connect the signal input from RF board AA1 to the signal output back to AA1.

Fast pulse modulator board - AA2/5

Servicing diagrams: Figs. 7-29 to 7-31.

Circuit functions

Fast pulse modulator board AA2/5 provides the following functions:-

- (1) High performance pulse modulation facility.
- (2) Step attenuation in five switchable stages with a total attenuation depth of 132 dB.
- (3) Reverse Power Protection (RPP) facility.

Fast pulse modulator board: Pulse mod (AA2/5 sheet 1)

Circuit diagram: Fig. 7-30.

Pulse modulation

The pulse modulator is designed using GaAs FET switch technology and is located before the step attenuator section. It is split into two identical sections which are separated by a metal wall in order to achieve high RF isolation. Each section is composed of two FET switches (ICs 4,5 and ICs 6,7) and a FET driver (IC8 and IC9). The FET devices are low insertion loss GaAs switches with each switch providing more than 20 dB of isolation at 2 GHz. These switches are controlled by a dedicated driver chip (IC8 and 9). The driver IC input comes from an external modulating source (50 Ω impedance) at TTL levels. When the level at input pin 4 is HIGH outputs at pins 1 and 8 are set to the voltages connected to pins 6 (+0.3 V) and 5 (-5 V) respectively, resulting in ICs 4 to 7 being switched to low insertion loss mode. When pin 4 goes LOW, the voltages on pins 1 and 8 are interchanged, which in turn puts switches ICs 4 to 7 into isolation mode. The delay from the time that the TTL level changes to switching the RF signal is less than 100 ns.

Relays RLA and RLB are used to select or bypass the pulse modulator circuit. These relays are latching type RF performance devices with high isolation and low insertion loss. Resistors R1 and R90 are used to terminate the 'open' contacts in order to maximise isolation further.

Amplifier

The single RF amplifying stage is located on the output port of the modulator and before the step attenuators. The amplifier is based on FET TR1. Its gain is set by R85, with R89 added to improve the output match. The DC biasing network is of a standard arrangement.

Fast pulse modulator board: RPP and atten (AA2/5 sheet 2)

Circuit diagram: Fig. 7-31.

Step attenuator

The attenuator section consists of five attenuating pads constructed from thick film resistors. There are three pads of 33 dB value and one each of 22 dB and 11 dB, giving a maximum attenuation depth of 132 dB. The four higher value pads consist of two Π resistor stages connected in series to facilitate the use of smaller value resistors, with lower parasitics, resulting in a flatter frequency response. These pads are switched with two separate relays in order to obtain greater isolation between the input and output of each pad. The 11 dB single relay pad is switched with a higher isolation type relay. All the relays are mounted on the ground side of the board and sit in individual 'pockets' in the RF module.

All relay control lines from RF board AA1 are decoupled using ceramic feedthrough Π filters. On some lines further decoupling is achieved by the addition of inductors L10 to L14 and capacitors C16 to C24 and C20. Diodes D11 to D15 are added to prevent damage to the relay drive circuitry on the RF board. Also two wall "intrusions" are introduced along the attenuator length to prevent surface wave propagation.

Reverse power protection

The Reverse Power Protection (RPP) consists of a reed-relay (RLM), capable of switching up to 50 W of RF power, with associated RF level detection and relay drive circuitry.

In normal operation the reed-relay contacts are closed and a small fraction of the RF voltage appears at the junction of R44 and R45. Both positive and negative RF voltage peaks are detected by the dual detector diode package D8. IC1 is a dual comparator package with open collector outputs. The peaks of the RF voltage waveform are detected by D8 and charge capacitors C8 and C9 to the peak RF level. When the voltage on C8, for a positive peak, becomes greater than the voltage threshold set on non-inverting input pin 3 of IC1a, the output of the comparator goes LOW switching TR1 OFF so that RLM becomes open circuit. In a similar fashion when C9 causes comparator IC1b non-inverting input pin 5 becomes more negative than inverting input pin 6, the output on pin 7 switches to the LOW state. The RPP trip status is indicated on the TRIP line. High voltage zener diode D9 is used to limit the coil EMF voltage and to keep this voltage relatively high in order to quickly discharge the magnetic field and thereby shorten the relay switching time.

In normal operation TR1 is ON and the RPP RESET line is set HIGH keeping TR2 in the OFF state. When an overload occurs TR1 switches OFF as described above. This allows the collector voltage of TR1 to feed back to the inverting input of comparator IC1b inverting input, clamping it at a voltage greater than 0 V. This has the desired effect of preventing the RPP relay from being reset even after the RF signal has been removed. Thereafter the RPP can only be reset by switching the RESET line LOW to switch on TR2, which, via IC1b, switches TR1 back into the ON state.

When an attenuator stage is switched between the two matched states, i.e. resistive pad or through line positions, the relay contacts momentarily become open circuit, creating a large standing wave. Inductors L15 and L16 are inserted to slow down these transients and thereby prevent false RPP trippers.

In order to keep board connections to a minimum, the +5 V line for the RPP circuit is generated locally using voltage regulator IC2.

Fast pulse and high power board - AA2/7

Servicing diagrams: Figs. 7-32 to 7-35.

Circuit functions

Fast pulse modulator board AA2/7 provides the following functions:-

- (1) High performance pulse modulation facility.
- (2) Step attenuation in five switchable stages with a total attenuation depth of 132 dB.
- (3) Switchable power amplifier stage with up to +25 dBm power output capability.
- (3) Reverse Power Protection (RPP) facility.

Fast pulse and high power board: Pulse mod (AA2/7 sheet 2)

Circuit diagram: Fig. 7-33.

Pulse modulation

The pulse modulator is designed using GaAs FET switch technology and is located before the step attenuator section. It is split into two identical sections which are separated by a metal wall in order to achieve high RF isolation. Each section is composed of two FET switches (ICs 204, 205 and ICs 206, 207) and a FET driver (IC208 and IC209). The FET devices are low insertion loss GaAs switches with each switch providing more than 20 dB of isolation at 2 GHz. These switches are controlled by a dedicated driver chip (IC208 and 209). The driver IC input comes from an external modulating source (50 Ω impedance) at TTL levels. When the level at input pin 4 is HIGH outputs at pins 1 and 8 are set to the voltages connected to pins 6 (+0.3 V) and 5 (-5 V) respectively, resulting in ICs 204 to 207 being switched to low insertion loss mode. When pin 4 goes LOW, the voltages on pins 1 and 8 are interchanged, which in turn puts switches ICs 204 to 207 into isolation mode. The delay from the time that the TTL level changes to switching the RF signal is less than 100 ns.

Relays RLA and RLB are used to select or bypass the pulse modulator circuit. These relays are latching type RF performance devices with high isolation and low insertion loss. Resistors R201 and R290 are used to terminate the 'open' contacts in order to maximise isolation further.

Amplifier

The single RF amplifying stage is located on the output port of the modulator and before the step attenuators. The amplifier is based on FET TR204. Its gain is set by R285, with R289 added to improve the output match. The DC biasing network is of a standard arrangement.

Fast pulse and high power board: Attenuator (AA2/7 sheet 3)

Circuit diagram: Fig. 7-34.

Attenuator

The attenuator section consists of five attenuating pads constructed from thick film resistors. There are three pads of 33 dB value and one each of 22 dB and 11 dB, giving a maximum attenuation depth of 132 dB. The four higher value pads consist of two Π resistor stages connected in series to facilitate the use of smaller value resistors, with lower parasitics, resulting in a flatter frequency response. These pads are switched with two separate relays in order to obtain greater isolation between the input and output of each pad. The 11 dB single relay pad is switched with a higher isolation type relay. All the relays are mounted on the ground side of the board and sit in individual 'pockets' in the RF module.

All relay control lines from RF board AA1 are decoupled using ceramic feedthrough Π filters. On some lines further decoupling is achieved by the addition of inductors L10 to L14 and capacitors C10 to C17 and C20. Diodes D9 to D13 are added to prevent damage to the relay drive circuitry on the RF board. Also two wall "intrusions" are introduced along the attenuator length to prevent surface wave propagation.

Fast pulse and high power board: Power amp & RPP (AA2/7 sheet 4)

Circuit diagram: Fig. 7-35.

Power amplifier

The power amplifier consists of two RF amplifying stages and an RF detector for approximate level indication. The first amplification stage is based around transistor TR1. Feedback resistor R55 and the emitter resistors R47 to R50 set the low frequency gain of this stage; with the values shown the gain is approximately 12 dB. The inductor chain L15 to L17 and L24 forms a broad band RF choke. The biasing condition for this stage is controlled by TR3. The base of TR3 is fixed at approximately 17 V, this sets the R57/L24 junction around 17.7 V. Resistors R56 and R57 in turn set the collector current to approximately 100 mA. The gain of the amplifier drops with increasing temperature. This effect can be minimized by a gradual reduction in the collector current of TR1 with increasing temperature. Diodes D14 and D15 and the thermistor R51 are used to produce this desired effect. When the temperature increases, TR3 base potential rises resulting in a decrease in TR1 collector current. The current variation is only around $\pm 10\%$ over the 0 to 55°C temperature range. 3 dB attenuator pad R44 to 46 is inserted to improve the amplifier input match and thereby reduce the level inaccuracy due to mismatch.

The output RF transistor stage biasing configuration for TR2 is very similar to that for TR1. The collector voltage is fixed at around +16 V and the collector current is nearly 300 mA. Temperature compensation on this stage is very subtle in order to maintain high power output, with only a few milliamps of current variation available from diode pair D16 and D17.

Components R69 and C36 are inserted to selectively improve the low frequency output match. Diode detector D18 detects RF signals down to around +5 dBm. The difference between the detected voltage and the 'dummy' detector (D22) voltage is amplified by the difference amplifier based around IC02a. The dummy detector provides offset and temperature compensation.

Reverse power protection

The Reverse Power Protection (RPP) consists of a reed-relay (RLM), capable of switching up to 50 W of RF power, with associated RF level detection and relay drive circuitry.

In normal operation the reed-relay contacts are closed and a small fraction of the RF voltage appears at the junction of R72 and R73. Both positive and negative RF voltage peaks are detected by the dual detector diode package D19. IC1 is a dual comparator package with open collector outputs. The peaks of the RF voltage waveform are detected by D19 and charge capacitors C39, C40 and C41, C42 to the peak RF level. When the voltage on C39 C40, for a positive peak, becomes greater than the voltage threshold set on non-inverting input pin 3 of IC1a, the output of the comparator goes LOW switching TR6 OFF so that RLM becomes open circuit. In a similar fashion when C41, C42 causes comparator IC1b non-inverting input pin 5 becomes more negative than inverting input pin 6, the output on pin 7 switches to the LOW state. The RPP trip status is indicated on the RPP TRIPPED line via R93. High voltage zener diode D20 is used to limit the coil EMF voltage and to keep this voltage relatively high in order to quickly discharge the magnetic field and thereby shorten the relay switching time.

In normal operation TR6 is ON and the RPP RESET line is set HIGH keeping TR9 in the OFF state. When an overload occurs TR6 switches OFF as described above. This allows the collector voltage of TR6 to feed back to the inverting input of comparator IC1b inverting input, clamping it at a voltage greater than 0 V. This has the desired effect of preventing the RPP relay from being reset even after the RF signal has been removed. Thereafter the RPP can only be reset by switching the RPP RESET line LOW to switch on TR9, which, via IC1b, switches TR6 back into the ON state.

When an attenuator stage is switched between the two matched states, i.e. resistive pad or through line positions, the relay contacts momentarily become open circuit, creating a large standing wave. Inductors L21 and L22 are inserted to slow down these transients and thereby prevent false RPP tripovers.

In order to keep board connections to a minimum, the +5 V line is generated locally using voltage regulator IC3.

Control board - AB1

Servicing diagrams: Figs. 7-36 to 7-51.

Introduction

This board contains the microprocessor, memory and audio frequency generator and provides all the instrument clocks as well as controlling and conditioning all the modulation signals ready for their use in the RF module. It also provides a serial communications link over which the RF module is controlled and it also supplies the RF module with the filtered power rails it requires. Finally, it interfaces with the front panel display, key pad and control knob and provides GPIB and RS-232 communications ports.

Control board: Microprocessor and memory (AB1 sheet 1)

Circuit diagram: Fig. 7-38.

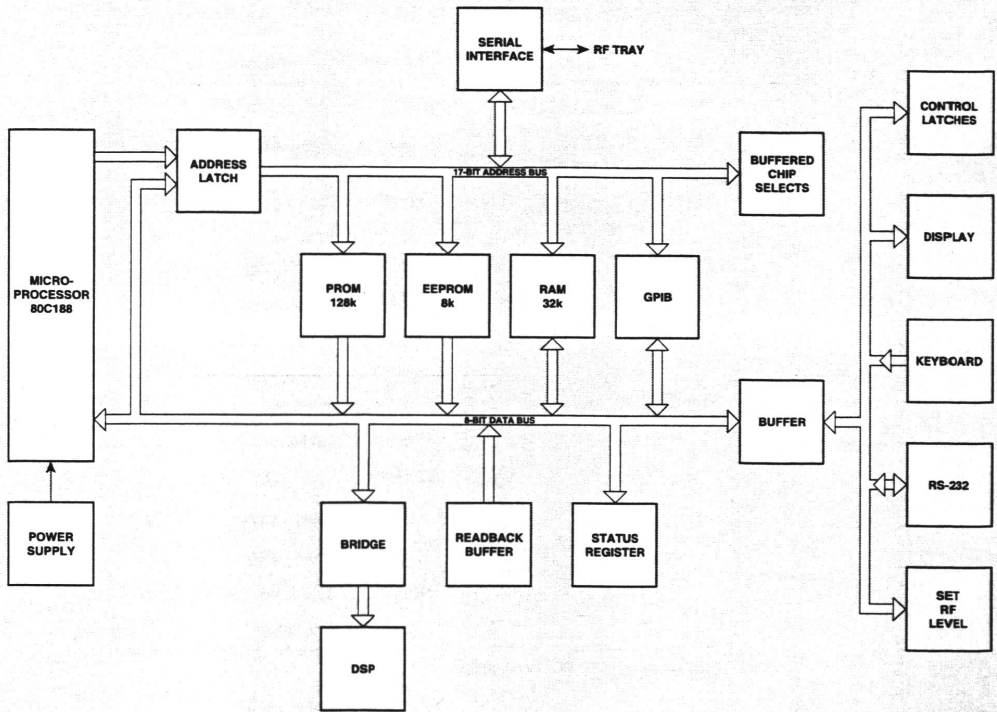
Microprocessor

Microprocessor IC2 which is used to control the instrument is an 80C188. It contains the CPU (Central Processor Unit) and several peripheral devices including an interrupt controller for 5 direct interrupt inputs, a DMA (Direct Memory Access) controller, timers and 7 programmable chip select outputs. The microprocessor uses an 8-bit data and a 20-bit address bus to address the memory. The data bus is multiplexed to provide either 8 bits of data or the lower 8 bits of the address. The block diagram of the phase locked loop is shown in Fig. 1-6.

Control signals TI0 and TI1 for the internal programmable timer and SRDY and ARDY for asynchronous/synchronous data transfer are tied high, the functions unused. TEST, HOLD and DRQ1 are disabled by being held low. The 20 MHz clock input, X1, is derived from the DSP 10 MHz clock output. Power supply monitoring circuitry provides the MRESET (L) signal to the microprocessor and a write inhibit signal MRESET (H) to EEPROM IC7 on power-up and also in the event of a power failure or brown-out situation occurring. This circuitry holds the microprocessor in reset at power-up long enough for the internal clock oscillator and the rest of the circuitry to stabilise. When released from reset the microprocessor retrieves and runs its program data from the instrument PROM, IC5.

WR (write) and RD (read) asserted low enable the memory or I/O device selected by the address bus to be written into or read out from respectively. DEN is the data enable line for the data bus buffer. PCS0 to PCS6 provide active-low Peripheral Chip Select signals. LCS and MCS provide chip select signals for RAM IC6 and EEPROM IC7 respectively. MCS3 provides a chip select signal for serial bus operation. TOUT1 provides a timing signal for the DSP. The RESET output is used to reset the GPIB controller.

The processor uses a multiplexed data bus to accommodate the 20-bit address. Output lines A8 to A19 carry the high order memory address. Input/output lines AD0 to AD7 carry the low order memory address during the first clock cycle and then carry data during the second and third machine state clock cycles. ALE (Address Latch Enable) is used to differentiate between data and address; when it is taken high the contents of the data bus are treated as part of the address and latched in IC4. ALE also latches A16 - A19 into IC3 in order to complete the 20-bit address. When ALE is taken low lines AD0 to AD7 carry data.



C2783

Fig. 1-6 Microprocessor and control block diagram

Interrupts

The 80188 has four interrupt inputs, INT0 to INT3. Interrupt INT0, the highest priority interrupt, is supplied by GPIB INT from the GPIB controller. INT1 is supplied from the RS-232 controller. INT2 is generated by the interrupt handler on the STAT_INT line to indicate that a status line has changed state. INT3 on the TRIGGER line is requested whenever an external trigger signal is applied to the TRIGGER socket on the rear panel.

The functions of the microprocessor interrupt inputs and the chip selects are summarised in Table 1-6 below:

Table 1-6: Interrupts and chip selects

INT0	GPIB interrupt	PCS0*	GPIB enable
INT1	RS-232 interrupt	PCS1*	Interrupt handler enable
INT2	Interrupt handler	PCS2*	Quiet bus enable
INT3	Trigger interrupt	PCS3*	DSP bridge enable
		PCS4*	Input buffer enable
NMI*	Knob interrupt	PCS5*	Trigger latch clear
		PCS6*	Serial bus control enable
		LCS*	RAM enable
		MCS0*	EEPROM enable
		MCS1*	Not used
		MCS2*	Not used
		MCS3*	Serial bus data enable
		UCS*	Not used

* indicates an active low signal

Memory bank

The operating program is contained in PROM (Programmable Read Only Memory) IC5. IC6 is the RAM (Random Access Memory) used for scratch-pad read/write operations. Unlike the other memory ICs which are non-volatile, the contents of the RAM are lost when the instrument is switched off. EEPROM (Electrically Erasable PROM) IC7 provides non-volatile storage for calibration data, user stores, etc. IC6 and IC7 are selected by chip select lines MCS0 and LCS respectively; IC5 is selected by address line A19. Memory bank addressing is summarised in Table 1-7 below.

Provision has been made for several different sizes of memory to be fitted as required, the sizes and types of memory catered for are shown below. The EPROM is fitted into a socket on the board to enable easy software upgrades.

Table 1-7: Memory bank addressing

EPROM, IC5	128k/ 256k/ 512k	A0-A18	addressed using the A19 line,
RAM, IC6	32k/ 128k	A0-A16	addressed using the LCS* line,
EEPROM, IC7	8k/ 32k	A0-A14	addressed using the MCS0* line.

Data transfer

On power-up or reset the processor transfers modulation setting data to the DSP using DMA (Direct Memory Access). Subsequent modulation settings are performed normally. Normal data transfer is done using the WR (write) and RD (read) lines.

All system switching, control and flag reads are done via a two-way buffer on the microprocessor bus. By this means the data bus following the buffer is free from the continuous data train of pulses on the normal microprocessor bus thus reducing the possibility of interference to the analogue circuits.

Control board: DSP audio generator (AB1 sheet 2)

Circuit diagram: Fig. 7-40.

The audio generator is based on Digital Signal Processor (DSP) IC12. This is booted up on power-up or reset from the microprocessor using a DMA dump of data to the DSP over a bridge. The bridge has two modes of operation, the first is used on power-up for the DMA memory dump and is controlled by BMS* and BR* on the DSP and by DRQ0 on microprocessor IC2. The second mode is used once the DSP has been booted up and is running normally, this uses DMS* on the DSP to control it.

On power-up the DSP BMS* line goes low to initiate the down-loading of data from the boot memory. This condition sets the output of D-type bistable IC11a to a high state, this line is tied to the DRQ0 input on the microprocessor so this line going high initiates a DMA memory dump to the DSP bridge. This entails the microprocessor down-loading a byte of data each time the DRQ0 line goes high. The BMS* line going low also sets the output of another D-type bistable, IC11b to a low state, this line is fed to the BR* input of the DSP causing the DSP to release control of the data bus and not read or write to it until the BR* line has returned high. When the microprocessor writes data to bridge latch IC10 it resets bistable IC11a output to a low and clocks bistable IC11b so that the output goes high. When the DSP sees the BR* line is high it does a read of the bridge using the BMS* line to enable the output of the bridge latch. This in turn sets in motion another cycle of the down-loading sequence. This cycle continues until the DMA down-load is completed. When it reaches the end of the DMA data the microprocessor ignores the next DRQ0 command and sends the start-up signal to the DSP.

Once the DMA down-load is completed the DSP bridge goes into its second mode of operation, namely that for normal operation. In this mode when data is written to the bridge latch using PCS3* and WR*, D-type bistable IC51b is clocked so that a high appears on the output. This line goes to the DSP to let it know that data has been written to the bridge, and also to data input latch IC1 which the microprocessor polls to see when the data has been read from the bridge. When the DSP sees this line go high it knows that data is waiting on the bridge and reads it from there using the RD* and DMS* lines, the RD* line enables the output of the bridge latch and the DMS* line resets the output of bistable IC51b to a low. When the bistable output goes low the microprocessor knows that the last data byte has been read and it can write the next data byte. In this way the microprocessor controls the DSP audio generator.

The DSP is used to generate the audio frequency signals which are used for internal modulation. It does this by outputting serial data on its serial port to 16-bit serial DAC IC13. The DAC output is then passed through filter chip IC14 which has been configured as an eighth-order Bessel low-pass filter with a 3 dB cut-off frequency of 20 kHz. After the filter the signal is buffered and amplified by IC15a to 2 V RMS and routed to the front panel from PLK (or to the rear panel via SKB if the rear-exit option is fitted). The filtered signal is also fed, via buffer IC15b, on the INTERNAL MOD line to the audio multiplexers (sheet 4).

The DSP uses the 10 MHz standard generated on the control board, but it also has a clock output line which outputs the 10 MHz clock with a 50% duty cycle. This clock output from the DSP is doubled to 20 MHz using a simple doubling circuit based on XOR-gate IC46b and an RC delay line (R150 and C7). The 20 MHz CLOCK is then used as the microprocessor clock input.

Trigger

The trigger input comes from SKA on the rear panel and is voltage protected to 50 V by series 10 k Ω resistors R4 and R8. This signal is active low and uses pull-up resistor R7 to +5 V to enable operation using a simple external switch. The input is routed to microprocessor IC2 to enable triggering of functions to be carried out, and to DSP IC12 where it is used as one of two FSK modulation data lines.

The trigger input to the microprocessor is fed via Schmitt inverter IC206d. The trigger input line to the DSP is buffered using OR-gate IC50c and is fed to the D17 data line of the DSP where it is used as the data input A for digital modulation.

Pulse modulation

The pulse modulation circuitry on the control board is limited to enabling or disabling the pulse modulation line and to determining whether an internal or external pulse modulation source is used.

The pulse modulation input comes from SKC on the rear panel and is voltage protected to 50 V by series 10 kΩ resistor R18. This input has a pull-down resistor, R17, to 0 V. The pulse modulation input line is buffered by OR-gate IC50d and is fed to the D18 data line of DSP IC12 where it is used as the data input B for FSK modulation.

Control board: Interrupts and serial interface (AB1 sheet 3)

Circuit diagram: Fig. 7-42.

Interrupt handler

The interrupt handler works around 8-bit magnitude comparator IC18 which compares eight live inputs with eight latched inputs. Latched inputs contain data written to interrupt handler latch IC17 by microprocessor IC2. Live inputs are interrupts from other parts of the control board circuitry. Only seven of the eight inputs are used, the eighth is tied low. When the two 8-bit inputs differ, an interrupt is generated which is fed to the INT2 input on the microprocessor. The microprocessor then reads interrupt handler input buffer IC19 to find out which input line has changed state. Before dealing with the interrupt the microprocessor writes this new data back to the interrupt handler latch to remove the interrupt at the microprocessor. When the interrupt has been dealt with, a second interrupt is generated which lets the microprocessor know that this input line is back in its normal state so it writes the original data back into the interrupt handler latch. The interrupt line to the microprocessor has a de-glitch circuit in it based around IC24a, R151 and C3, this ensures that the live input to the interrupt handler is an interrupt and not just a momentary glitch on one of the interrupt lines. The interrupt handler is addressed using the PCS1* chip select line. Inputs to the interrupt handler are shown in Table 1-8 below.

Table 1-8: Interrupt lines

Name	Function
D0	ALC HI
D1	ALC LO
D2	OXCXO HI
D3	OXCXO LO
D4	EXT STD DETECT
D5	KBRD INT
D6	SERIAL BUS INT
D7	Not used

Serial bus

There are two serial buses generated on the control board, the first is a buffered serial bus used to control the RF module and the second is a local serial bus which is used on the control board for controlling octal DAC IC34. The serial bus is made up of three lines, a data line down which the serial address and data is sent, a clock line which synchronizes the data recovery and an enable line which enables the receiving devices on the other end of the serial link when data is being transmitted.

The serial bus data line is fed from two parallel-to-serial shift registers onto which the data and address bytes are loaded. The serial output of data register IC21 is fed into the serial input of address register IC23, so when the two shift registers are clocked together the address and then the data are sent down the data line of the serial bus one after the other. The clock and enable

lines for both the local and RF module serial buses are provided by latch IC22. This latch also clocks the data through the shift registers and onto the serial data line. All the RF module serial bus lines and the data line of the local serial bus are buffered using tri-state buffers IC28. The buffers on the RF module clock and enable lines are permanently enabled, and the buffers on both of the serial buses data lines can be individually enabled using serial bus latch IC22. By being able to tri-state the data line of the RF module serial bus it enables this line to be used to read back a data bit from the location addressed. This serial bit is read in on data input latch IC1 addressed using PCS4*. The serial bus latch is addressed using PCS6* and the shift registers are addressed using MCS3*.

Buffered data bus and control lines

Certain devices on the control board require a buffered data bus and buffered control lines, i.e. lines that remain quiet when not in use. The data bus is buffered using bi-directional tri-state buffer IC27 which has pull-down resistors R185 to R192 to ground on the quiet side of the buffer. The control lines buffered are A0, A1, A2, RD* and WR* and they are buffered using OR-gates IC16 and IC9b. Also, extra chip select lines are required for the buffered devices, these are provided by address decoder IC20 which provides an extra eight buffered chip select lines. The buffered lines and chip selects are all addressed on PCS2*.

The control lines supplied by buffered hardware control latches IC25 and IC26 are shown in Table 1-9 below.

Table 1-9: Latch control lines

IC25		IC26	
Q0	1 MHz/10 MHz	Q0	not used
Q1	INT/EXT	Q1	φM/FM
Q2	PLL/DAC	Q2	AM S0
Q3	AC/DC	Q3	AM S1
Q4	DSP RESET*	Q4	AM S2
Q5	INT PULSE ENABLE	Q5	FM S0
Q6	EXT PULSE ENABLE	Q6	FM S1
Q7	INT STD OUT	Q7	FM S2

The buffered chip select lines are used to address the functions shown in Table 1-10 below.

Table 1-10: Buffered chip selects

Line	Signal	Function
Y0	BCS0*	Keyboard interface enable
Y1	BCS1*	LCD display enable
Y2	BCS2*	RS-232 interface enable
Y3	BCS3*	Dual 12-bit DAC IC35 enable
Y4	BCS4*	Control latch IC25 enable
Y5	BCS5*	Control latch IC26 enable
Y6	BCS6*	Dual 12-bit DAC IC3 update
Y7	BCS7*	Knob interface enable

Control board: Modulation and level (AB1 sheet 4)

Circuit diagram: Fig. 7-44.

External modulation input

This input (PLL or optionally SKE) has a nominal input impedance of 100 k Ω in the standard version of the instrument, although provision has been made to enable a 600 Ω input impedance version to be offered as an option by fitting R155 and R156. This input can be either AC or DC coupled by opening or closing relay RLA by means of the AC/DC line to TR1. From here the signal is reduced from the nominal 1 V RMS input voltage to 1 V pk-pk using potential divider R203 and R204. It is then passed from buffer IC30a either directly to the modulation conditioning circuitry or through an ALC circuit to be levelled to 1 V pk-pk. The ALC circuit works by using variable resistor TR6 to adjust the gain of amplifier IC48. The variable resistor is voltage controlled by a pair of positive and negative peak detectors based around D12 and C27, and D14 and C28 whose outputs are averaged to reduce errors induced by complex waveforms. The ALC output is monitored by a window comparator formed by IC47a, b and d to provide out-of-range signals on the ALC HI and ALC LO lines to the microprocessor.

Composite modulation

The composite modulation signal basically sums, with equal weighting, the internal and external modulation signals and feeds the result on for use in either the AM or FM/ ϕ M modulation paths. The external modulation signal summed is the direct input signal.

The signals on the INTERNAL MOD and EXT MOD DIRECT PATH are summed into the inverting input of operational amplifier IC38a through resistors R133 and R134. The output from this operational amplifier is fed into the inverting input of IC38b which inverts the signal again and adjusts its amplitude to 1 V pk-pk.

Amplitude modulation

Analogue multiplexer IC31 can feed a number of sources onto the AM modulation signal path. The sources available are external modulation direct, external modulation ALC, internal modulation, 1 V calibration voltage, composite modulation or ground. Voltage divider R102 and R103 provide the 1 V calibration voltage via IC38c.

After the multiplexer the signal is buffered and has its amplitude adjusted for losses in this path by operational amplifier IC33a. It then passes through 12-bit DAC IC35b which sets the depth-of-modulation (range 0 to 4000) in 0.1% steps. The DAC has a maximum output of 99.9% with 100% being equal to 1 V pk. After this the signal path splits into two.

The first path can have a DC voltage offset applied to it by the b-section of 8-bit octal DAC IC34. The signal then passes through a square law correction circuit based on IC33c and TR4 and is then amplified by IC33d before being passed out to the RF module as the AM signal. The AM square law correction circuit is adjusted using the a-section of octal DAC IC34.

The second path can have a DC offset applied to it by the c-section of octal DAC IC34. The signal is then amplified by IC37a and fed to 12-bit DAC IC35a which sets the RF level (range 40 to 4000) in 0.1 dB steps. After the DAC the signal passes through a square law correction circuit, based on IC37c and TR5, which can be adjusted using the d-section of octal DAC chip IC34. Finally, it is routed to the RF module via amplifier IC37d as the RF LEVEL REF signal.

Frequency/Phase modulation

The FM/ ϕ M path can be fed a signal from a number of sources by analogue multiplexer IC32. The sources available are external modulation direct, external modulation ALC, internal modulation, 1 V calibration voltage, composite modulation or ground.

After the multiplexer the signal can be either amplified to 1.4 V pk and routed to the RF module via PLD as the FM signal, or it can pass through a differentiator circuit, which has a slope of 6 dB/octave, and be passed on to the RF module as the ϕ M signal. Analogue switch IC29b is used to determine which path is selected. The FM or ϕ M conversion is done by a high output current operational amplifier, IC49b, which is required to drive the load on the RF module.

Control board: Standard selection (AB1 sheet 5)

Circuit diagram: Fig. 7-46.

Clock circuitry

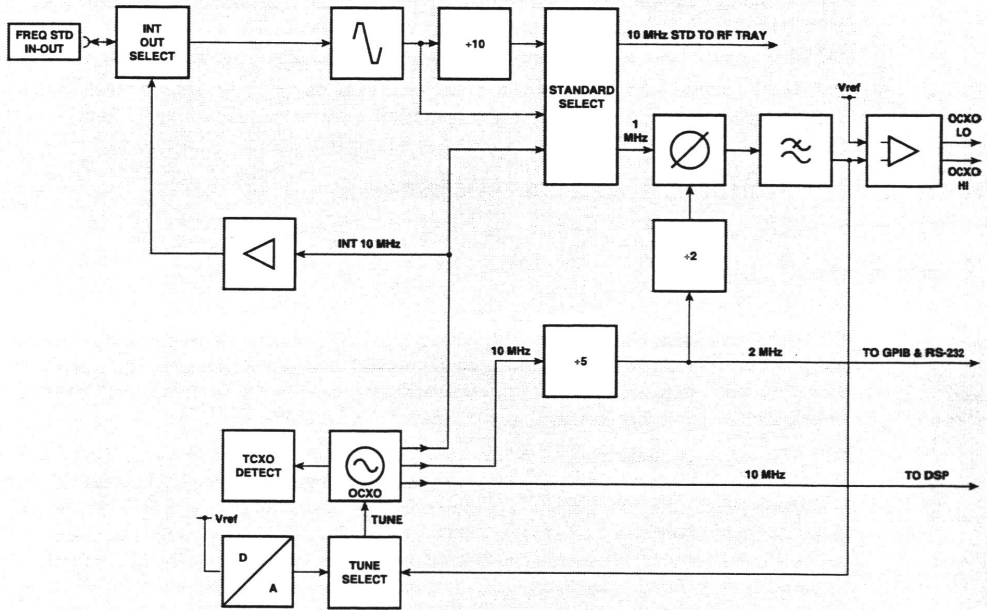
This includes the internal 10 MHz standard, which supplies 10 MHz to the control board and the RF module, and which is divided down to provide a 2 MHz clock for the GPIB interface and the RS-232 serial link. It also includes the external standard conditioning circuitry and phase locked loop (PLL) circuitry to allow the internal oscillator to be phase locked to an external 1 MHz or 10 MHz clock. Frequency standard selection is summarised in Fig. 1-7.

The +5 V supply for all the clock circuitry is locally regulated down from the +11 V rail using regulator IC59. This is required to prevent noise from the digital circuitry on the standard +5 V rail causing jitter in the PLL when it is in operation. The control board has a dual oscillator footprint on it to allow either a 10 MHz OCXO or a 10 MHz TCXO to be used as the internal oscillator; which option is fitted can be read back on data input latch IC1. The signal from oscillator X1 is buffered using inverters IC45, and then routed to the DSP and to the RF module via switch IC42. When enabled by INT STD OUT, IC62 also directs the internal standard to the rear panel FREQ STD IN-OUT socket via SKF. The 10 MHz is also divided by five using IC61a to provide a 2 MHz clock for the GPIB and the RS-232 interfaces. This 2 MHz clock is then further divided by two using IC61a to produce a 1 MHz clock with 50% duty cycle which is used to clock one half of the PLL circuit.

The PLL circuit based on IC44a, b and IC43a, b takes two inputs at 1 MHz, one derived from the internal standard and one from the external standard, and generates a voltage output which varies according to the phase difference between the two inputs. Two output voltages are produced by this circuit because the OCXO and the TCXO require tuning voltages with opposite senses to make them phase lock correctly. If the tuning voltage gets too high or too low an appropriate OCXO HI or OCXO LO out-of-range signal is generated using the window detector based round comparators IC43c and d. This tuning voltage is applied to the oscillator voltage control input to adjust the frequency output accordingly. When the PLL circuit is not in operation a fixed tuning voltage can be applied to the oscillator using switch IC36. The fixed tuning voltage is generated using the f-section and g-section of octal DAC IC34. These generate a tuning voltage with a range of +1 V to +4 V which is set during calibration in the factory. Voltage divider R178 and R179 provide the reference voltage via IC47c for the DAC.

The circuit automatically detects if a TCXO or an OCXO is fitted by monitoring the current supply to the TCXO Vcc input. When the OCXO is fitted there is only the quiescent current of IC60 passing through the current sense resistor R205 and this is not enough to generate the voltage drop required to turn on transistor TR8, so the TCXO DETECT line is held low. When the TCXO is fitted the voltage drop across R205 causes TR8 to turn on, which pulls the TCXO DETECT line to +5 V. The TCXO DETECT line is fed to input buffer IC1 (sheet 1), and also to IC36 where it is used to automatically route the tuning voltage from the PLL.

The external standard first passes through some conditioning circuitry based on TR2 and TR3 which ensures that it is at the correct logic levels when it is passed on to the rest of the circuitry. It can then either be routed directly to switch IC42 or it can be divided by ten using IC41a and then routed to the switch; it is at this stage that the external signal is detected using TR7. Switch IC42 is used to route the external standard to one of the PLL inputs either directly if the external standard is 1 MHz or after it has been divided by ten if it is a 10 MHz external standard. Switch IC42 is used to route either the 10 MHz external standard or the 10 MHz internal standard as required to the RF module.



C2736

Fig. 1-7 Frequency standard selection

Control board: Interface (AB1 sheet 6)

Circuit diagram: Fig. 7-48.

GPIB

The GPIB interface is provided using a standard chipset consisting of GPIB controller IC56 and transceivers IC57 and IC58. The +5 V GPIB power supply is locally filtered by L1, C34 and R145 to prevent noise leakage out of the instrument. The controller is addressed using PCS0*, and the GPIB interrupt is fed into the INT0 input of microprocessor IC2 (sheet 1). A 2 MHz clock is provided which enables the controller to internally derive the transfer rate of the link. The GPIB signal lines are fed from the controller through the transceivers to the board-mounted rear panel GPIB connector SKP.

RS-232

The RS-232 serial link is provided by one of the two serial interfaces present in asynchronous communications controller IC53. The controller is supplied with a 2 MHz clock which enables it to internally derive the baud rate of the link. This IC uses the buffered data bus and control lines to prevent noise leakage from the instrument. The RS-232 serial link is addressed using BCS2*, and the RS-232 interrupt is fed to the INT1 input on microprocessor IC2 (sheet 1). The RS-232 lines are fed through multiple driver and receiver IC52 before going to the board-mounted rear panel RS-232 connector SKR. The driver and receiver IC contains the three output drivers and the five input receivers that are required for the RS-232 link.

Knob

The knob signals come from the front panel on a 40-way ribbon cable which plugs into PLH on the control board. These signals are generated by an optical shaft encoder on the front panel and are in phase quadrature with each other; the direction of rotation of the knob can be determined

by detecting the sequence of changes of these two signals. This is done using the second serial interface on the asynchronous communications controller IC53. The CTS1* and the DSR1* inputs are the only two lines used on this serial interface, the rest are tied low. When either of these two lines changes state an interrupt is generated, this interrupt is fed into the NMI* input on microprocessor IC2. The microprocessor then reads the serial interface internal buffer, using BCS7*, and compares this new data with the last reading taken to determine the direction of rotation of the knob.

Key pad

The key pad is driven by the parallel port on asynchronous communications controller IC53 and is addressed using BCS0*. Eight data lines, Y0 to Y7, are used as outputs to hold the columns of the key pad low and the ERR*, SLCT, BUSY, PE and ACK* lines are used as inputs to read the five rows of the key pad. These five input lines have pull-up resistors to +5 V to hold them high unless a key is pressed. They are also fed into eight-input NAND-gate IC54 which generates an interrupt signal whenever one of its inputs is pulled low. One of the remaining three input lines to the NAND-gate is connected to the INIT* line of the IC53 parallel port and is used as an interrupt enable line (the remaining two NAND-gate inputs are pulled high). The keyboard interrupt is routed to the interrupt handler which then generates an interrupt on INT2 of microprocessor IC2. When an interrupt is received the microprocessor first reads which row is pulled low and then switches all eight data line outputs high and pulses them low in turn to determine which column is being used, in this way the microprocessor can read which key is being pressed on the key pad.

Front panel display

The front panel LCD display requires two connectors. The first connector provides power for the cold cathode fluorescent lamp used to illuminate the LCD display and is provided by an inverter module in the power supply area of the instrument. The second connector provides all the logic signals and power supplies for the LCD display itself, and these all come from the control board.

The contrast voltage for the LCD display has a voltage range of about -11 V to -7 V and is generated using the h-section of octal DAC chip IC34. The voltage from the DAC can vary between -3 V and +3 V, this is then conditioned and temperature compensated by comparator IC55a, a thermistor and resistors R125 to R129. The thermistor is positioned on the front panel PCB to detect the temperature at the display. The display uses the buffered data bus and is addressed using BCS1*.

Control board: PSU filtering and regulation (AB1 sheet 7)

Circuit diagram: Fig. 7-50.

Power for the control board and for the RF module enters the control board from the switched mode power supply on the PLN connector, it is then filtered and smoothed and routed appropriately. The power supply rails are monitored to detect power rail failure or brown-out (incipient power failure) conditions. In either of these events microprocessor IC2 is put into reset and EEPROM IC7 is inhibited from being written to.

The power supplies required on the control board are +5 V, ± 11 V and a stable +5 V reference voltage. The power supplies delivered to the RF module, via the PLD connector, are +24 V, +21 V, ± 11 V, +5 V, +5 V_{clean} and +5 V_{fracn}.

The +5 V supply is only used for the digital circuitry on the control board and is taken off directly from the power supply input with only filtering by C232 and C234 applied to it. It is further filtered by L205, C213, C235 and C236 before going to the RF module. The +5 V_{fracn} supply is separately filtered (by L207, C221 and C204) from the standard +5 V line and is used to power only the fractional-N divider on the RF board. The +5 V_{ref} voltage required by the control board is supplied by voltage reference IC204 powered from the +24 V rail. The +5 V (clean) voltage supply required on the RF module is regulated down from the +12 V rail using regulator IC203.

The +11 V rail is regulated down from the +12 V input from the switched mode power supply using a low-drop regulator based around IC205a, R212, R213 and TR201. Filtering is provided by L206, C211 and C231. Additional filtering for the +11 V rail is provided by L203 and C215 to C219 before it is used on the RF module.

The -11 V rail is not regulated and so is only approximately -11 V, it relies on the voltage drop across transistor TR202 to set the level of this voltage rail. TR202 is used in conjunction with L201, C205 and C208 to actively filter this rail before use on the control board. Additional filtering for the -11 V rail is provided by L204, C202, C225, C226 and C227 before it is used on the RF module.

The +24 V rail is initially filtered by C203, C204 and C228, and is further filtered by L202 and C206 before being used on the RF module. The +24 V rail is also routed to voltage regulator IC201 where it is regulated down to +21 V for use on the RF module. Output filtering is provided by C207 and C209.

IC201, IC203 and TR201 are all mounted on heatsinks to prevent damage by overheating at higher temperatures. The heatsinks also allow operation at ambient temperature with no air flow over the board, such as might occur during servicing.

Processor reset

The microprocessor monitoring circuit, based around comparator IC202, provides a reset signal to microprocessor IC2 and a write inhibit signal to EEPROM IC7 (sheet 1). It does this on power-up and also in the event of a power failure or brown-out (incipient power failure) situation occurring on the +5 V supply rail. This circuit holds the microprocessor in reset at power-up long enough for the internal clock oscillator and the rest of the circuit to stabilise.

It does this by monitoring the +5 V and +24 V power rails and asserting the reset line if the voltage on either of these rails falls beneath a pre-determined level. The monitoring circuit is made up of open-collector output comparators IC202a and IC202b. These are powered off the +12 V and 0 V rails, and have their outputs wire-ORed together through R222 and R226. The combined output is then pulled up to the +12 V rail via R223 which combines with capacitor C233 to give a power-on delay. The reset output is prevented from going too high by being clamped to +5 V by diode D206. The signal is then fed to the input of Schmitt-trigger inverter IC206b.

The non-inverting input to the first comparator, IC202a, comes from the +5 V power rail through 1 k Ω resistor R218. The negative input is the +5 V REF rail voltage divided down to about 4.6 V by R220 and R221. This ensures that if the +5 V rail is less than about +4.6 V the reset line will be pulled LOW.

The non-inverting input of the second comparator, IC202b, has a pull-down resistor to 0 V and has 15 V zener diode D207 tying it to the +24 V rail; this holds this input at about +9 V. The inverting input of this comparator is tied directly to the +5 V REF rail. This ensures that if the +24 V rail is less than +15 V, the reset line will be pulled LOW. The +24 V power rail has to be included in the reset circuit because the +5 V REF line, which is used as the reference for the +5 V rail comparator, is powered from it. If the +24 V rail voltage drops, reset will be asserted when it reaches about +20 V, which ensures that the +5 V REF is still being generated.

If the +12 V rail goes down the comparators lose their power supply and pull-up resistor R223 pulls the reset line LOW instead of the comparators.

Control board: Power supplies (AB1 sheet 8)

Circuit diagram: Fig. 7-51.

Power supplies

This sheet shows the board power supply table. All unused ICs are also shown.

Backlight inverter board - AC1

Servicing diagrams: Figs. 7-52, 53.

This board performs two functions: the first is to provide the cold cathode fluorescent tube on the display with its power, the second is to provide a filtered power supply to the fan.

The cold cathode fluorescent tube is powered by DC-to-AC inverter module X1. This requires a power supply of +5 V which is filtered by C1 to C4 and L1 before being fed into the inverter module. Output from the module at PLCB is a 450 V RMS sinusoidal waveform at a frequency of 30 kHz.

A +5 V fan is used (as opposed to the more usual +12 V fan) to prevent noise from the fan being introduced onto the +12 V rail, used for the more sensitive analogue areas of the instrument. The power supply for the fan is filtered by L2, L3 and C5, C6. The fan requires a maximum current of 165 mA.

Front panel - AF1

Servicing diagram: Fig. 7-54.

The front panel is a replaceable unit and therefore no technical description is given. The unit does not include the control knob encoder, cables or display LCD. If a fault occurs with the unit it is recommended that the complete unit is replaced. However, as an aid to fault finding, the keyboard circuit diagram is given under AF1 in Chap. 7, together with front panel access and removal instructions which are given in Chap. 2.

AC power supply

Servicing diagram: Fig. 7-1.

The AC power supply is a replaceable unit and therefore no technical description is given. If a fault occurs with the unit it is recommended that the complete unit is replaced. However, as an aid to fault finding, the power supply connections are shown on the interconnection diagram in Chap. 7, together with unit removal instructions which are given in Chap. 2. The DC outputs are additionally identified in Chapter 4.

AC/DC power supply

Circuit diagrams: Figs. 7-55 to 7-59.

The power supply module is a switched mode design which operates from both an AC supply of 94 to 264 V, 45 to 440 Hz or a DC supply of 11 to 32 V. The battery charging facility is not used in this instrument. Fig. 1-8 shows a block diagram of the AC/DC power supply module.

The circuits of the instrument require the supplies shown in Table 1-11 below.

Table 1-11: Power supplies

+5 V	2.8 A
+12 V	2.3 A
-12 V	0.6 A
+24 V	0.6 A output

The AC supply enters the instrument through a connector on the rear panel and passes through a fuse and two poles of a triple pole, double throw on/off switch. The supply then enters the power supply module where it is fed to a bridge rectifier in the AC-DC converter to produce an unregulated DC supply. The voltage of this depends on the supply voltage as the full range of AC input voltage is covered without range switching.

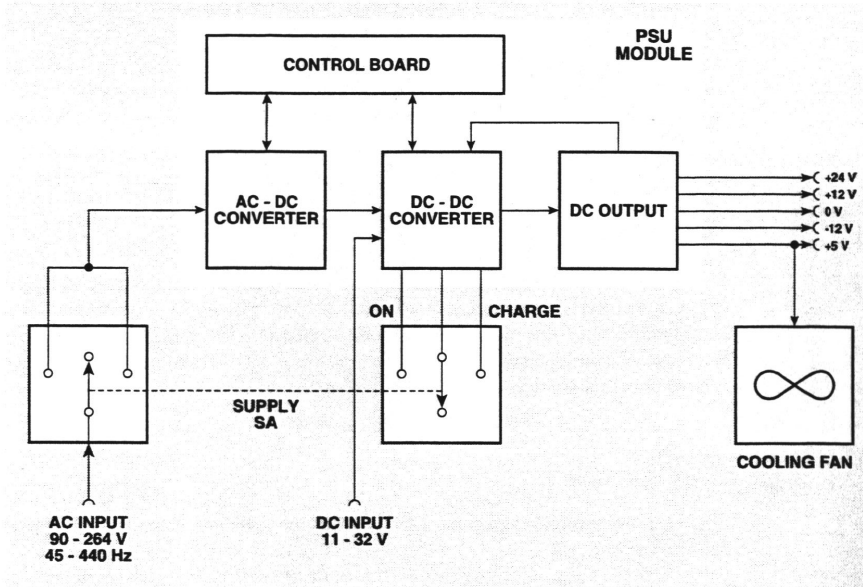
The second stage of the AC-DC converter produces semi-regulated DC supplies of 24 V using a 60 kHz switched mode oscillator and transformer coupling. This transformer also provides the safety isolation barrier.

TECHNICAL DESCRIPTION

The DC external or the DC supply from the AC-DC converter is used to drive the DC-DC converter.

The DC output circuits producing the four regulated output supplies are each fed from an individual winding on the DC-DC converter output transformer.

Regulation is applied to the DC-DC converter from the output current and voltage sensing circuits.



C2798

Fig. 1-8 Block diagram of AC/DC power supply module (the charging facility is not used in this instrument)

Current monitoring to provide regulation is obtained from the three common-return supplies and voltage monitoring from the +5 V supply.

The 24 V supply has a voltage regulator configured within it.

A control circuit PCB contains the components for frequency control and regulation of both converters.

The third pole of the power on-off switch is connected to the DC-DC converter circuits through plugs and sockets.

Chapter 2

MAINTENANCE

Contents

General precautions	2-2
Chip components	2-2
Bulkhead connectors and gasket	2-2
Torque settings	2-2
Access to units and boards	2-3
Access for servicing	2-3
Removal of instrument cover	2-3
Access to board AA1	2-3
Access to boards AA2	2-3
Access to board AB1	2-3
Access to PSU and board AC1	2-3
Access to keyboard and display	2-6
Removal of units and boards	2-6
Removing RF tray	2-6
Removing front panel	2-6
Removing AC power supply unit	2-6
Removing AC/DC power supply unit	2-6
Removing board AA1	2-8
Removing board AA2, AA2/1, AA2/5 and AA2/7	2-8
Removing board AA2/2	2-8
Removing board AB1	2-8
Removing board AC1	2-9
Routine maintenance	2-9
Safety testing and inspection	2-9

List of figures

Fig. 2-1	Standard instrument - View from above with instrument cover removed	2-4
Fig. 2-2	Standard instrument - View from below with instrument cover removed	2-4
Fig. 2-3	Standard instrument - View from above with PSU cover and front panel removed ..	2-5
Fig. 2-4	AC/DC option - View from above with PSU cover and front panel removed	2-5
Fig. 2-5	Standard instrument - View of RF tray with cover removed	2-7
Fig. 2-6	Standard instrument - View of attenuator tray with cover removed	2-7

General precautions

Chip components

Numerous chip capacitors and resistors are fitted in this instrument. These have silver palladium end cap terminations with nickel barriers. When soldering these devices the following precautions should be observed:

- (1) Use a low melting point solder, and a soldering iron set to 315°C (600°F). The use of a high wattage soldering iron will minimise the time taken to solder the device.
- (2) Take care to avoid mechanical damage from flexing the PCB.

Static sensitive components

The CMOS integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges (see preliminary pages, 'Precautions'). Boards that have such integrated circuits all carry warning notices against damage by static discharge. Take care also when using freezer sprays to aid fault finding. These can create a static charge likely to change the programmed memory of (E)PROMs.

Bulkhead connectors and gasket

To ensure that no RF leakage occurs all bulkhead connectors and lid sealing gaskets must be securely fitted. It is essential that the unit lids are correctly relocated in their slotted recesses after removal and all the screw type connectors are tightened up to their specified torque (see 'Torque settings' below).

Torque settings

Unless otherwise stated it is imperative that when replacing semi-rigid pipe connections the following torque setting is used:

SMA : 99 TO 106

Unless otherwise stated all screws have the following torque setting:

70 Ncm

Access to units and boards

The procedures below follow the order of access for servicing then removal of units and boards.

Access for servicing

Removal of instrument cover

Before any servicing of the instrument can be performed, the instrument cover must be removed as follows:

- (1) Remove 4 M4 screws from the side panels, 2 each side adjacent to the front panel handles.
- (2) Remove 2 M3 screws holding the cover to the rear panel.
- (3) Remove 2 M4 screws, one from each rear stand-off.
- (4) Remove the case by pulling it to the rear.

Ensure that when refitting the rear panel gasket is not damaged.

Access to board AA1

Turn the instrument upside down to gain access to the underside. A view of the instrument from below is shown in Fig. 2-2. Remove 25 M3 × 6 mm screws on the periphery of the RF tray cover then remove the remaining, 22 M3 × 20 mm screws holding the cover to the RF screens. Remove the tray cover, which exposes the top surface of double-sided RF board AA1.

When refitting take care that the gaskets are correctly fitted and undamaged.

Access to boards AA2

To gain access to these boards, first of all remove board AB1 (see 'Removing AB1 board' below) to expose the attenuator cover. Remove the cover after removing 22 M3 screws (torque setting 50 Ncm). A view of the attenuator tray with cover removed is shown in Fig. 2-6.

When refitting the cover take care that the gasket is correctly fitted and undamaged.

Access to board AB1

Removing the instrument cover gives immediate access from above to control board AB1. A view of the instrument from above showing board AB1 is given in Fig. 2-1.

Access to PSU and board AC1

Removing the power supply cover gives access to the power supply unit and backlight inverter board AC1. Remove the cover after removing 11 M3 screws. Views of the instrument from above with the power supply cover removed are shown in Fig. 2-3 for the AC power supply and in Fig. 2-4 for the optional AC/DC power supply.

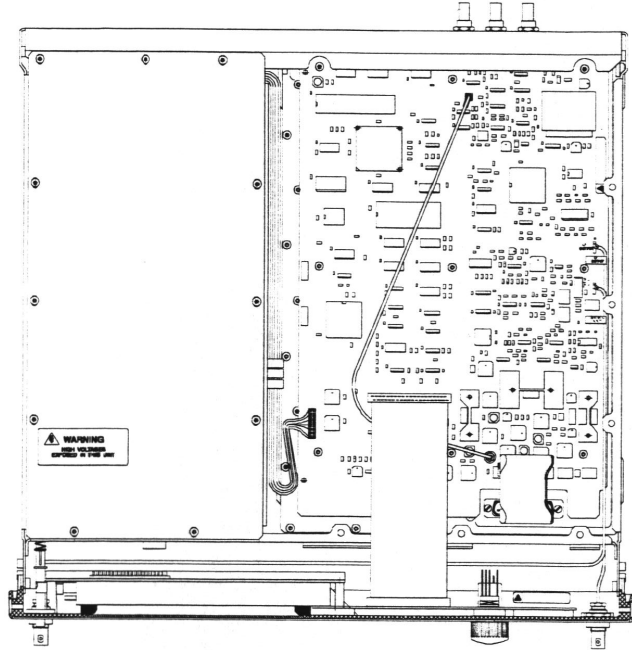


Fig. 2-1 Standard instrument - View from above with instrument cover removed

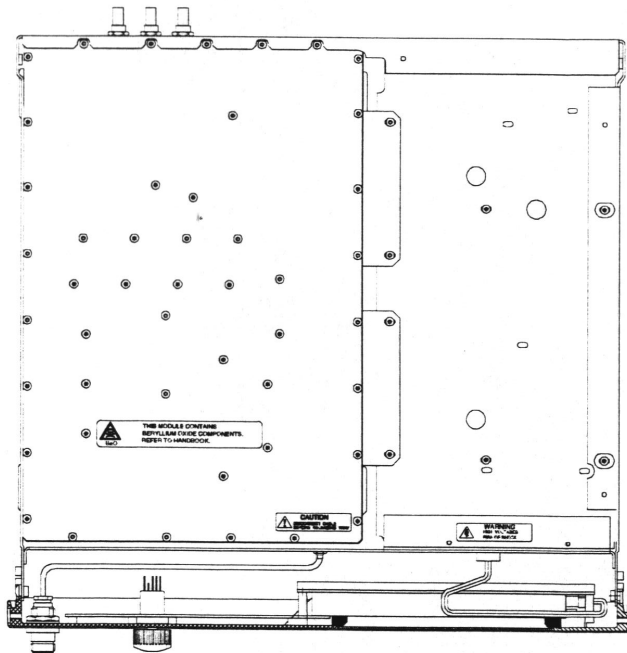


Fig. 2-2 Standard instrument - View from below with instrument cover removed

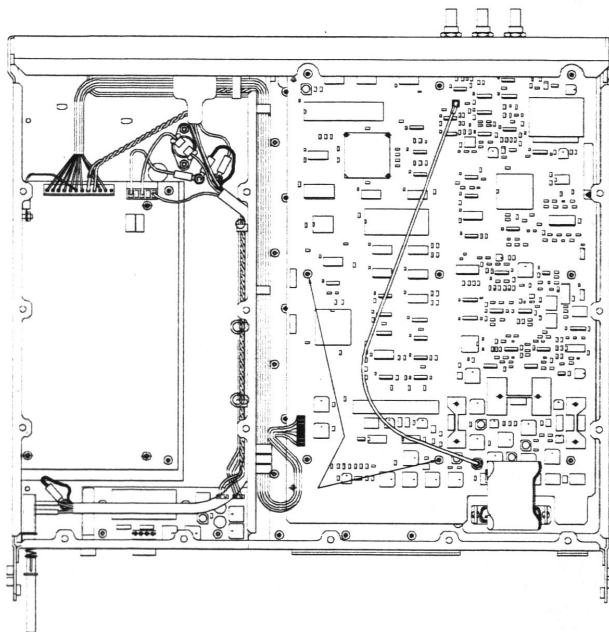


Fig. 2-3 Standard instrument - View from above with PSU cover and front panel removed

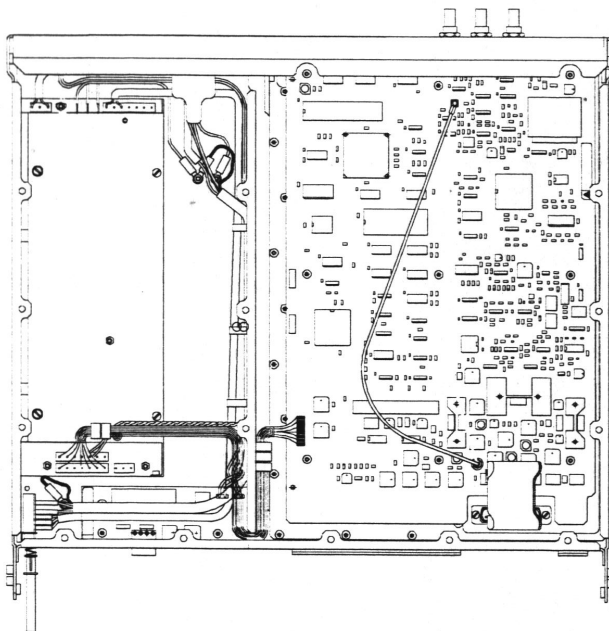


Fig. 2-4 AC/DC option - View from above with PSU cover and front panel removed

Access to keyboard and display

Access to the front panel boards is gained after removing the front panel (see 'Removing front panel' below) from the instrument. Figs. 2-1 and 2-2 show the positions of the boards.

Removal of units and boards

Removing RF tray

Before removing the RF tray, board AB1 must be removed (see 'Removing AB1 board' below). Then proceed as follows:

- (1) Remove the 4 sideframe screws holding the tray.
- (2) Turn the instrument upside down and unscrew the semi-rigid RF OUTPUT cable at the RF tray end. (The torque setting at the front panel end is 1.6 Nm.)
- (3) Remove the 4 screws from the two side plates connecting to the PSU.
- (4) Remove the 2 screws connecting to the rear panel. Remove the tray.

Removing front panel

Proceed as follows:

- (1) Disconnect the semi-rigid cable at the RF tray end.
- (2) Pull off the following connectors:
 - (a) Ribbon cable connector to PLH labelled TO FRONT PANEL on board AB1.
 - (b) Connector to PLL labelled EXT MOD I/F on board AB1.
 - (c) Connector to PLK labelled LF OUT on board AB1.
 - (d) Front panel power supply connector at the PSU end after first pressing the catch underneath the connector to release it.
- (3) Release the front panel by removing 4 M4 screws (torque setting 1.6 Nm), 2 each side of the front panel. Pull the front panel forwards so that the hole in the panel clears the SUPPLY switch. Make sure that the flexible cables are free.

When refitting the semi-rigid cable use a torque of 1.0 Nm at the RF tray end.

Removing AC power supply unit

Remove the power supply cover (see 'Access to PSU and board AC1' above). A view of the instrument from above with the power supply cover removed is shown in Fig. 2-3 . Then proceed as follows:

- (1) Pull off the 2 connectors to the board.
- (2) Unscrew and remove the earthing tag.
- (3) Remove 2 side panel screws.
- (4) Remove 4 screws from underneath the instrument. The complete unit can now be lifted out.

Removing AC/DC power supply unit

Remove the power supply cover (see 'Access to PSU and board AC1' above). A view of the instrument from above with the power supply cover removed is shown in Fig. 2-4 . Then proceed as follows:

- (1) Pull off the 3 multi-way connectors at the front of unit.
- (2) Pull off the 2 multi-way connectors at the rear of unit.
- (3) Pull off the 3 single connectors at the rear , noting the colour and position of each: red to +ve, black to -ve, green/yellow to E.

- (4) Remove 10 screws (5 on bottom, 5 at side) securing the unit to the main frame. The complete unit can now be lifted out.

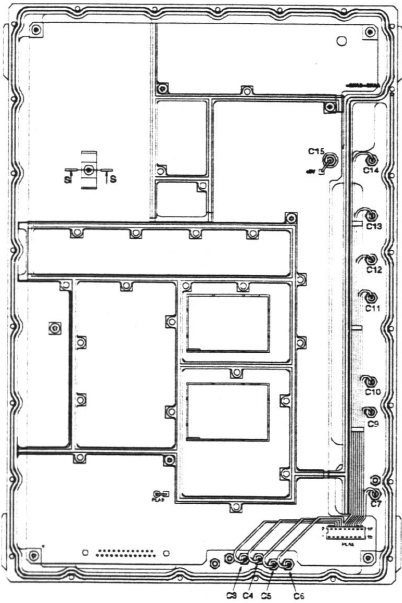


Fig. 2-5 Standard instrument - View of RF tray with cover removed

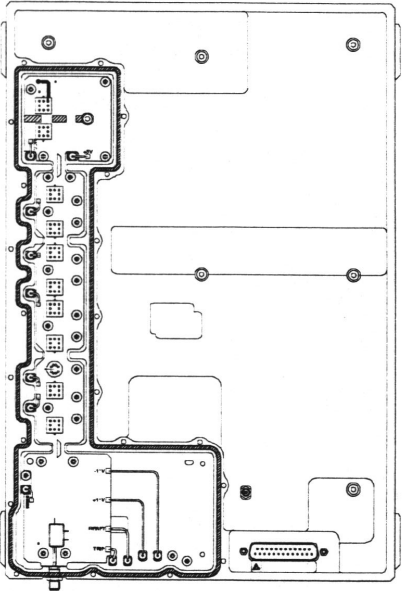


Fig. 2-6 Standard instrument - View of attenuator tray with cover removed

To obtain access to the PCBs within the unit, remove the 4 screws holding the protective cover in place, then remove the cover.

Removing board AA1

Remove the RF cover (see 'Access to board AA1' above). A view of the RF tray with cover removed showing board AA1 is given in Fig. 2-5 . Then proceed as follows:

- (1) Remove the 4 M3 × 8 mm screws holding the amplifier and synthesizer RF screens in place and remove the screens together with their gaskets.
- (2) Unsolder PLAB and one feed-through in a cut-out on the board.
- (3) Unplug PLAE.
- (4) Unscrew and remove the pillar holding the sprung earth contact.
- (5) Unsolder SKAA and SKAD at the junction of the inner and outer wall.
- (6) Unscrew the studmounts for PLAC from the other side of the tray.
- (7) Unscrew and remove the 4 screws at the outer corners of the board and one near the board edge. Remove the board.

When replacing the board, remember to refit the connector gasket.

Removing board AA2, AA2/1, AA2/5 and AA2/7

Remove the attenuator cover (see 'Access to boards AA2' above). Then proceed as follows:

- (1) Unsolder 12 feed-throughs (15 for AA2/1 and AA2/7) at the board ends.
- (2) Unsolder the connection to the RF O/P SMA socket.
- (3) Unsolder the RF input and pulse input connections.
- (4) Remove 2 M2.5 screws either side of TR2 on AA2/1 and AA2/7.
- (5) Remove 23 M3 screws (25 for AA2/1 and AA2/7) and lift out the board.

Removing board AA2/2

Remove the attenuator cover (see 'Access to boards AA2' above). Then proceed as follows:

- (1) Unsolder the connection to the RF O/P SMA socket.
- (2) Unsolder the RF input and pulse input connections.
- (3) Remove 12 M3 screws and lift out the board.

Removing board AB1

Proceed as follows:

- (1) Unscrew and remove the nuts holding each of the rear panel BNC sockets.
- (2) Unscrew and remove the fastenings holding the RS232 and IEEE 488.2 connectors to the rear panel.
- (3) Pull off the following board connectors:
 - (a) Connector to PLL labelled EXT MOD I/P.
 - (b) Connector to PLK labelled LF OUT.
 - (c) Connector to PLN labelled FROM POWER SUPPLY.
 - (d) Ribbon cable connector to PLH labelled TO FRONT PANEL.
 - (e) Connector to PLG, 10 MHz standard at the RF tray end.
- (4) Unscrew and pull off the ribbon cable connector to PLD labelled TO RF TRAY at the RF tray end.
- (5) Remove 9 M3 screws holding the board to the RF tray. Lift the board out whilst sliding it forward so that the rear connectors clear the cutouts in the rear panel.

For servicing purposes the control board may be removed and operated, still connected to the instrument by its cables. After board removal insert the board fingers in the bracket provided at the display end of the main frame (the bracket can be seen in Figs. 2-3 and 2-4.)

Removing board AC1

Remove the power supply cover (see 'Access to PSU and board AC1' above). Then proceed as follows:

- (1) Pull off the front panel power supply connector at the PSU end after first pressing the catch underneath the connector to release it.
- (2) Pull off the fan supply connector PLCA.
- (3) Pull off the power supply connector PLCC.
- (4) Unscrew and remove 4 M3 board holding screws and lift out the board.

Routine maintenance

Safety testing and inspection

In the UK, the 'Electricity at Work Regulations' (1989) section 4(2) places a requirement on the users of equipment to maintain it in a safe condition. The explanatory notes call for regular inspections and tests together with a need to keep records.

The following electrical tests and inspection information is provided for guidance purposes and involves the use of voltages and currents that can cause injury. It is important that these tests are only performed by competent personnel.

Prior to carrying out any inspection and tests, the instruments must be disconnected from the mains supply and all external signal connections removed. All tests should include the instrument's own supply lead, all covers must be fitted and the equipment supply switch must be in the 'ON' position.

The recommended inspection and tests fall into three categories and should be carried out in the following sequence:-

1. Visual inspection
2. Earth bonding tests (Class I equipment only)
3. Insulation resistance test

1. Visual inspection

A visual inspection should be carried out on a periodic basis. This interval is dependent on the operating environment, maintenance and use, and should be assessed in accordance with guidelines issued by the Health and Safety Executive (HSE). As a guide, this instrument when used indoors in a relatively clean environment would be classified as 'low risk' equipment and hence should be subject to safety inspections on an annual basis. If the use of the equipment is contrary to the conditions specified, you should review the safety re-test interval.

As a guide, the visual inspection should include the following where appropriate:

Check that the equipment has been installed in accordance with the instructions provided (e.g. that ventilation is adequate, supply isolators are accessible, supply wiring is adequate and properly routed).

The condition of the mains supply lead and supply connector(s).

Check that the mains supply switch isolates the instrument from the supply.

The correct rating and type of supply fuses.

Security and condition of covers and handles.

Check the supply indicator functions (if fitted).

Check the presence and condition of all warning labels and markings and supplied safety information.

Check the wiring in re-wireable plugs and appliance connectors.

If any defect is noted this should be rectified before proceeding with the following electrical tests.

2. Earth bonding tests

Earth bonding tests should be carried out using a 25 A (12 V maximum open circuit voltage) DC source. Tests should be limited to a maximum duration of 5 seconds and have a pass limit of 0.1Ω after allowing for the resistance of the supply lead. Exceeding the test duration can cause damage to the equipment. The tests should be carried out between the supply earth and exposed case metalwork, no attempt should be made to perform the tests on functional earths (e.g. signal carrying connector shells or screen connections) as this will result in damage to the equipment.

3. Insulation resistance test

A 500 V DC test should be applied between the protective earth connection and combined live and neutral supply connections with the equipment supply switch in the 'ON' position. It is advisable to make the live/neutral link on the appliance tester or its connector to avoid the possibility of returning the instrument to the user with the live and neutral poles linked with an ad-hoc strap. The test voltage should be applied for 5 seconds before taking the measurement. IFR products employ reinforced insulation in their construction and hence a minimum pass limit of $7 \text{ M}\Omega$ should be achieved during this test.

Where a DC power adapter is provided with the instrument, the adapter must pass the $7 \text{ M}\Omega$ test limit.

We do not recommend dielectric flash testing during routine safety tests. Most portable appliance testers use AC for the dielectric strength test which can cause damage to the supply input filter capacitors.

4. Rectification

It is recommended that the results of the above tests are recorded and checked during each repeat test. Significant differences between the previous readings and the measured values should be investigated.

If any failure is detected during the above visual inspection or tests, the instrument should be disabled and the fault should be rectified by an experienced Service Engineer who is familiar with the hazards involved in carrying out such repairs.

Safety critical components should only be replaced with equivalent parts, using techniques and procedures recommended by IFR Ltd.

The above information is provided for guidance only. IFR products are designed and constructed in accordance with International Safety Standards such that in normal use they represent no hazard to the operator. IFR Ltd reserves the right to amend the above information in the course of continuing its commitment to product safety.

Chapter 3

ADJUSTMENT PROCEDURES

Contents

Introduction	3-3
Test equipment.....	3-3
Warm-up time.....	3-3
Unlocking procedure.....	3-3
Resetting the password.....	3-3
Adjustments.....	3-4
Menu operation.....	3-4
Adjusting calibration data	3-4
Date setting and calibration exit.....	3-4
Recommended test equipment	3-5
Adjustment procedures	3-6
1 Synthesiser (self-calibration).....	3-6
2 Prediction factor.....	3-6
3 Frequency standard	3-6
4 Ext mod reference	3-7
5 Int mod offset.....	3-8
6 Int mod amplitude.....	3-8
7 FM factor	3-9
8 Unlevelled mod	3-9
9 FM tracking (self-calibration).....	3-10
10 Levelled (ALC) mod.....	3-10
11 PM factor	3-11
12 RF level.....	3-12
13 AM	3-13
14 AM flatness.....	3-13
15 RF level (normal system).....	3-14
16 Pulse system level.....	3-14
17 Attenuator pads (not required for units fitted with Option 1)	3-15
Adjustment procedures for instruments fitted with Option 3 or 11.....	3-16
18 High power RF level.....	3-16
19 High power pulse system level.....	3-16
Adjustment procedure tables	3-19
Option 3 or 11.....	3-24

List of tables

Table 3-1 Recommended test equipment	3-5
Table 3-2 UTIL 102 Frequency standard adjustment	3-19
Table 3-3 UTIL 103 Ext mod reference adjustment	3-19
Table 3-4 UTIL 104 Int mod offset adjustment.....	3-19
Table 3-5 UTIL 105 Int mod amplitude adjustment	3-19
Table 3-6 UTIL 106 FM factor adjustment	3-20
Table 3-7 UTIL 107 Unlevelled mod adjustment	3-20
Table 3-8 UTIL 109 Levelled (ALC) mod adjustment.....	3-20
Table 3-9 UTIL 110 PM factor adjustment	3-20
Table 3-10 UTIL 111 RF level adjustment.....	3-20
Table 3-11 UTIL 112 AM adjustment	3-20
Table 3-12 UTIL 113 AM flatness adjustment.....	3-21
Table 3-13 UTIL 114 RF level (normal system).....	3-21

contd./...

List of tables *(continued)*

Table 3-14 UTIL 115 Pulse system level	3-22
Table 3-15 UTIL 118 Attenuator pads (not Option 1).....	3-23
Table 3-16 UTIL 116 High power RF level (normal system)	3-24
Table 3-17 UTIL 117 High power pulse system level.....	3-25

List of figures

Fig. 3-1 Frequency adjustment test set-up.....	3-7
Fig. 3-2 Ext mod reference adjustment test set-up	3-7
Fig. 3-3 Unlevelled mod adjustment test set-up	3-9
Fig. 3-4 Modulation adjustment test set-up.....	3-10
Fig. 3-5 Modulation adjustment test set-up.....	3-11
Fig. 3-6 RF output test set-up	3-12

Introduction

This chapter describes adjustments which will restore the instrument to its peak operating condition. Test equipment recommended for this purpose is listed in Table 3-1 below and summarized before each adjustment procedure. All the routine adjustments for the instrument can be carried out from the front panel.

Test equipment

To ensure minimum errors and uncertainties when making measurements, it is important to always use recently calibrated test equipment, with any correction figures taken into account, so as to establish a known traceable limit of performance uncertainty. This uncertainty must be allowed for in determining the accuracy of measurements.

Warm-up time

Allow all instrument to warm up for at least 30 minutes before commencing adjustments.

Unlocking procedure

In order to access the adjustment routines it is necessary to unlock the instrument to Level 2 by pressing:

[MENU]

80 [ENTER]

Select *Level 2*: and enter the six digit password (the default password is 123456)

Resetting the password

To reset the password unlock the instrument then press:

[MENU]

81 [ENTER]

Select *Set Level 2 Password*: and enter the six digit password.

ENSURE THAT A RECORD OF THE MODIFIED PASSWORD IS KEPT.

For this purpose it is recommended that the adjustment form at the end of this chapter is duplicated and the modified password recorded on the duplicate.

Adjustments

If more than one adjustment is to be performed, they must be performed in the order below.

The adjustments are as follows:

UTIL 100	Synthesiser	
UTIL 101	Prediction factor	
UTIL 102	Frequency standard	
UTIL 103	Ext mod reference	
UTIL 104	Int mod offset	
UTIL 105	Int mod amplitude	
UTIL 106	FM factor	
UTIL 107	Unlevelled mod	
UTIL 108	FM tracking	
UTIL 109	Levelled (ALC) mod	
UTIL 110	PM factor	
UTIL 111	RF level	
UTIL 112	AM	
UTIL 113	AM flatness	
UTIL 114	Normal system level	
UTIL 115	Pulse system level	
UTIL 116	High power system	(Units fitted with Option 3 or 11)
UTIL 117	High power & pulse	(Units fitted with Option 3 or 11)
UTIL 118	Attenuator pads	(Not units fitted with Option 1)
UTIL 119	Set calibration date	

To ensure that the adjustment remains in specification throughout the calibration period it is advisable to ensure that the figures remain within the limits stated at the beginning of each section.

Menu operation

The [MENU] key selects the main utility menu, or within utility menus steps back up through the menus.

The [PREV] key is used to scroll backwards through a menu list.

The [NEXT] key is used to scroll forwards through a menu list.

The [SELECT] key selects an item highlighted on a utility menu.

Adjusting calibration data

This can be achieved in most cases by using the rotary control or single stepping using the [x10 ↓] and [+10 ↑] keys. Alternatively, a number can be entered using the keypad terminated by the [ENTER] key.

If any DAC adjustment value falls outside 10% limits from either end of the DAC range (*i.e.* <25 or >230 in the case of an 8 bit DAC) then investigate the measurement further to ensure that a fault condition does not exist.

Date setting and calibration exit

Before carrying out any adjustments, the date may be set such that when selecting *Save cal data and quit* after the appropriate adjustment has been *successfully* completed, the date of the adjustment will be recorded. Selecting *Quit without saving cal data* (which may be used if a calibration has been unsuccessful), will not set the new date or save any data.

To set the current date select UTIL 119, Set Calibration Date, and enter the date in the form YYYY MM DD; the dashes are automatically inserted.

Recommended test equipment

The test equipment recommended for these procedures is shown below. Alternative equipment may be used provided it complies with the stated minimum specification.

Table 3-1 Recommended test equipment

Description	Minimum specification	Example
Power meter	± 0.1 dB from 10 kHz to 2.4 GHz	IFR* 6960B with 6912 Sensor
Modulation meter	AM, FM and Φ M 50 kHz to 2.4 GHz. Accuracy $\pm 1\%$ at 1 kHz modulation frequency	IFR* 2305
Digital voltmeter Counter	DC voltage measurement 10 kHz to 2.4 GHz frequency range	Solartron 7150+ EIP 535B or IFR* 2440

*IFR Ltd was previously known as Marconi Instruments Ltd

Adjustment procedures

Each adjustment procedure relies on the UUT being set to its power-up conditions. To avoid switching the instrument off and back on, reset the UUT by selecting:

[RCL] 999 [ENTER]

At the end of this chapter are a set of adjustment forms. These tables should be photocopied and used to record the data values of all the adjustments made.

Adjustments for the options, where necessary, are included with the tests for the standard instrument, with the exception of Options 3 and 11 (High Power and High Power + Fast Pulse Modulation respectively) which have a dedicated chapter.

1 Synthesiser (self-calibration)

No test equipment required

The synthesiser calibration resets the VCO presteer DAC values and realigns the voltage tuned filters (both on the AA1 RF board).

- (1) Select:
- | | |
|----------|-------------|
| [MENU] | 100 [ENTER] |
| [SELECT] | |

This calibration will only take about 10 seconds.

- (2) Select the appropriate calibration exit.

2 Prediction factor

No test equipment required

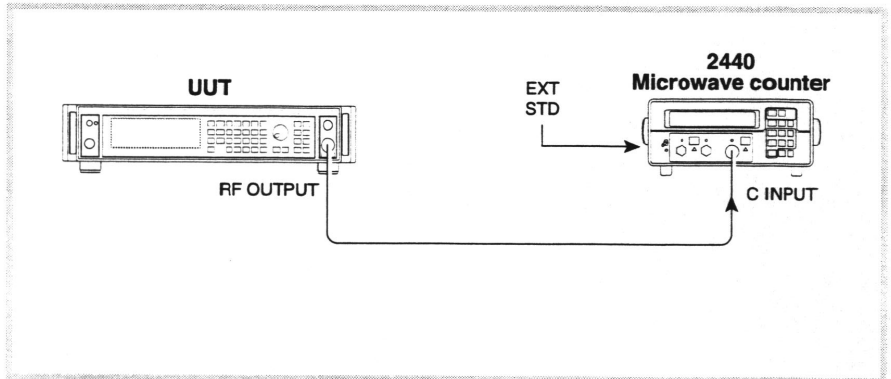
The prediction factor is set in the factory with default data and requires no further adjustment. In the event of this data becoming corrupted or an EEPROM change, the default prediction factor to be entered is 8.

3 Frequency standard

Test equipment

Description	Minimum specification	Example
Counter	10 Hz to 2.4 GHz	EIP 535B or IFR 2440

Adjustment procedure



C2738

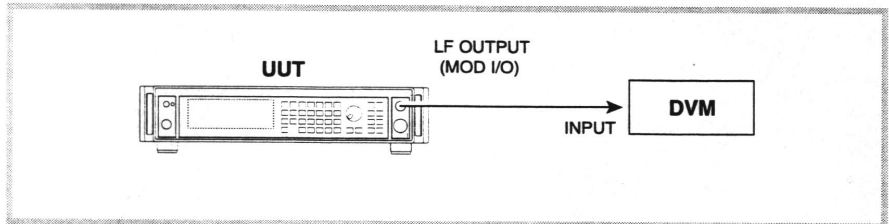
Fig. 3-1 Frequency adjustment test set-up

- (1) Apply an external frequency reference to the counter and connect the test equipment as shown in Fig. 3-1.
 - (2) On the UUT select:
[MENU] 102 [ENTER]
- Adjust the coarse DAC then the fine DAC until a frequency as close as possible to 2400 MHz is displayed on the counter.
- (3) Select the appropriate calibration exit.

4 Ext mod reference

Test equipment

Description	Minimum specification	Example
Digital voltmeter	DC voltage measurement	Solartron 7150+



C3870

Fig. 3-2 Ext mod reference adjustment test set-up

This sets the output level of the DSP audio generator to provide an accurate DC level from the LF OUTPUT (MOD I/O for instruments fitted with Option 7 or 11) socket for the purpose of Unlevelled mod adjustment (Section 8).

- (1) Connect the test equipment as shown in Fig. 3-2.
- (2) Set the digital voltmeter to read DC volts.

7 FM factor

Test equipment

Description	Minimum specification	Example
Counter	10 Hz to 2.4 GHz	EIP 535B or IFR 2440

Adjustment procedure

This provides the overall FM accuracy adjustment. In DC FM mode, the UUT is internally set 100 kHz below the displayed frequency so the adjustment at the carrier frequency is setting the 100 kHz deviation.

- (1) Apply an external frequency reference to the counter and connect the test equipment as shown in Fig. 3-1.
- (2) On the UUT select:

[CARR FREQ]	1 [GHz]
[RF LEVEL]	0 [dB]
[MENU]	106 [ENTER]

Adjust the FM Factor DAC until a frequency as close as possible to 1000 MHz is displayed on the counter.

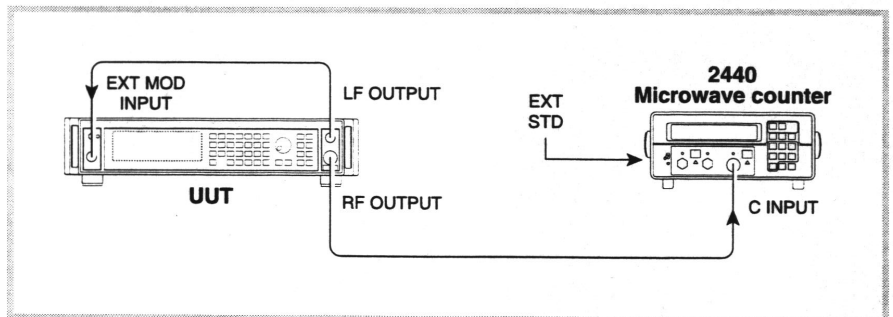
- (3) Select the appropriate calibration exit.

8 Unlevelled mod

Test equipment

Description	Minimum specification	Example
Counter	10 Hz to 2.4 GHz	EIP 535B or IFR 2440

Adjustment procedure



C2740

Fig. 3-3 Unlevelled mod adjustment test set-up

This establishes a value to load into the ALC DAC such that 1 V RMS applied to the EXT MOD INPUT socket gives the same voltage as internal and levelled external.

Notes

Ext Mod Reference (Section 4) and FM Factor (Section 7) must precede this adjustment.

The connection shown between EXT MOD INPUT and LF OUTPUT (on the standard instrument) is not required for instruments fitted with Option 7 or 11. With these Options the signal is routed internally.

- (1) Apply an external frequency reference to the counter and connect the test equipment as shown in Fig. 3-3.
- (2) On the UUT select:

[CARR FREQ]	1 [GHz]
[RF LEVEL]	0 [dB]
[MENU]	107 [ENTER]

Adjust the Mod Amplitude DAC until a frequency as close as possible to 1000 MHz is displayed on the counter.
- (3) Select the appropriate calibration exit.

9 FM tracking (self-calibration)

No test equipment required

This will ensure that the FM deviation is the same at all carrier frequencies and modulation rates. It does not set the accuracy; this is performed by the FM Factor adjustment in Section 7.

- (1) Select:

[MENU]	108 [ENTER]
[SELECT]	

This calibration will only take about 10 seconds.

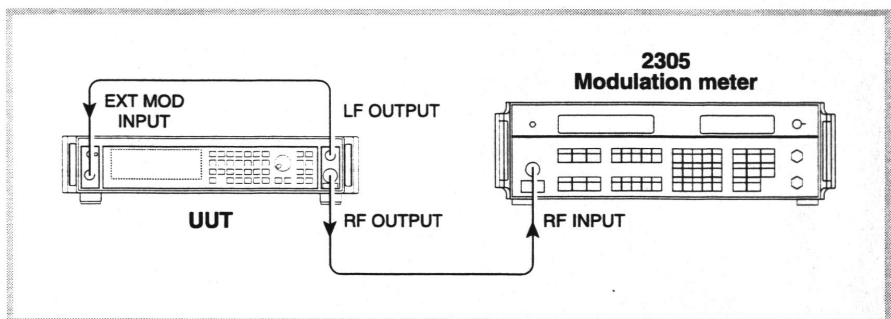
- (2) Select the appropriate calibration exit.

10 Levelled (ALC) mod

Test equipment

Description	Minimum specification	Example
Modulation meter	FM accuracy $\pm 1\%$ at 1 kHz modulation frequency	IFR 2305

Adjustment procedure



C2741

Fig. 3-4 Modulation adjustment test set-up

Notes

Notes

The connection shown between EXT MOD INPUT and LF OUTPUT (on the standard instrument) is not required for instruments fitted with Option 7 or 11. With these Options the signal is routed internally.

- (1) Connect the test equipment as shown in Fig. 3-4.
- (2) On the modulation meter, select CAL, FM, 50 Hz \Rightarrow 15 kHz filter.
- (3) On the UUT set:

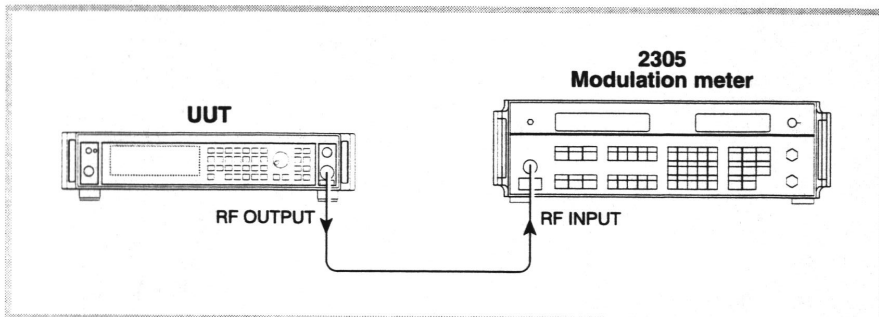
[CARR FREQ]	1 [GHz]
[RF LEVEL]	0 [dB]
[MENU]	109 [ENTER]

Measure the FM deviation on the modulation meter. Select Mod Source to Ext ALC (by pressing 1) and adjust the ALC DAC until the Ext ALC FM deviation equals the Internal deviation.

- (4) Select the appropriate calibration exit.

11 PM factor**Test equipment**

Description	Minimum specification	Example
Modulation meter	FM accuracy $\pm 1\%$ at 1 kHz modulation frequency	IFR 2305

Adjustment procedure

C2742

Fig. 3-5 Modulation adjustment test set-up

This provides the overall phase modulation accuracy adjustment.

- (1) Connect the test equipment as shown in Fig. 3-5.
- (2) On the modulation meter, select CAL, FM, 50 Hz \Rightarrow 15 kHz filter.
- (3) On the UUT select:

[CARR FREQ]	1 [GHz]
[RF LEVEL]	0 [dB]
[MENU]	110 [ENTER]

Adjust the PM Factor DAC until a deviation as close as possible to 10.00 kHz is displayed on the modulation meter.

- (4) Select the appropriate calibration exit.

13 AM**Test equipment**

Description	Minimum specification	Example
Modulation meter	AM accuracy $\pm 1\%$ at 1 kHz modulation frequency	IFR 2305

Adjustment procedure

This provides the overall amplitude modulation accuracy adjustment.

- (1) Connect the test equipment as shown in Fig. 3-5.
- (2) On the modulation meter, select CAL, AM, 50 Hz \Rightarrow 15 kHz filter.
- (3) On the UUT select:
[MENU] 112 [ENTER]

The UUT will be set to 0 dBm with 30% AM on a 300 MHz carrier.

Adjust DAC A until the AM reading displayed on the modulation meter is as close as possible to 30%.

- (4) On the UUT select *AM Depth* and press 1 to set 80%.
- (5) Enter the AM depth measured on the modulation meter into the UUT.
- (6) Adjust DAC B for the AM depth now indicated by the UUT.
- (7) The adjustment of DAC B will affect DAC A and vice versa. so it will be necessary to repeat steps (3) and (6) until no further adjustment is necessary.
- (8) Select the appropriate calibration exit.

14 AM flatness**Test equipment**

Description	Minimum specification	Example
Modulation meter	AM accuracy $\pm 1\%$ at 1 kHz modulation frequency	IFR 2305

Adjustment procedure

This is required to take out any depth errors between the AM levelling loop and the final output levelling loop. As the AM loop has a bandwidth of more than 50 kHz and the levelling loop has a bandwidth of less than 1 kHz, measurement of the mod. depth above and below 1 kHz is made.

- (1) Connect the test equipment as shown in Fig. 3-5.
- (2) On the modulation meter, select CAL, AM, 30 Hz \Rightarrow 50 kHz flat filter.
- (3) On the UUT select:
[MENU] 113 [ENTER]

The UUT will be set to 0 dBm with 40% AM (at 3 kHz) on a 300 MHz carrier.

Measure the AM depth (nominally 40%).

- (4) On the UUT press 1 to select 50 Hz modulation frequency.

Adjust DAC until the AM reading displayed on the modulation meter is the same as that measured in step (3) above.

- (5) Select the appropriate calibration exit.

Adjust Cal Factor until the reading displayed on the power meter is as close as possible to +2.00 dBm (or +7.00 dBm for instruments fitted with Option 7 or 11).

- (4) On the UUT select subsequent Cal Points in turn, adjusting the Cal Factor at each step until the reading displayed on the power meter is as close as possible to +2.00 dBm (or +7.00 dBm for instruments fitted with Option 7 or 11).

17 Attenuator pads (not required for units fitted with Option 1)

Test equipment

Description	Minimum specification	Example
Power meter	± 0.1 dB from 30 kHz to 2.4 GHz	IFR 6960B with 6912 Sensor

Adjustment procedure

This adjustment sets up a calibration value for each attenuator pad at each frequency point. The overall RF frequency responses must be adjusted first. Cal Point 0 is at 10 MHz, Cal Point 1 is at 120 MHz and the remaining cal points are in 120 MHz steps up to 1.2 GHz (2023) or 2.4 GHz (2024).

Each pad is represented by a number; 0 = 33 dB, 1 = 11 dB, 2 = 33 dB, 3 = 22 dB, 4 = 33 dB.

- (1) ZERO and AUTOCAL the power meter.
- (2) Connect the test equipment as shown in Fig. 3-6.
- (3) On the UUT select:
[MENU] 118 [ENTER]

The UUT will be set to approximately +15 dBm at 10 MHz (Cal Point 0)

- (4) Set a reference on the power meter and AVERAGE 5 ENT.
- (5) Select *In/Out Pad* and press 1 to insert pad 0.

Select *Measured Atten* and enter the reading on the power meter to two decimal places (e.g. 33.14 [ENTER]).

- (6) Deselect pad 0.
- (7) Select pads 1 to 4 in turn repeating steps (5) and (6) above.
- (8) Select Cal Points 1 to 20 in turn repeating steps (4) to (7) above.

Adjustment procedures for instruments fitted with Option 3 or 11

18 High power RF level

Test equipment

Description	Minimum specification	Example
Power meter	±0.1 dB from 30 kHz to 2.4 GHz	IFR 6960B with 6912 Sensor

Adjustment procedure

This adjustment sets up the overall RF frequency response in 60 MHz steps. Cal Point 0 is at 10 MHz, Cal Point 1 is at 60 MHz and the remaining cal points are in 60 MHz steps up to 1.2 GHz (2023) or 2.4 GHz (2024).

- (1) ZERO and AUTOCAL the power meter.
- (2) Connect the test equipment as shown in Fig. 3-6.

- (3) On the UUT select:

[MENU] 116 [ENTER]

The UUT will be set to +19 dBm at 10 MHz (Cal Point 0)

Adjust Cal Factor until the reading displayed on the power meter is as close as possible to +19.00 dBm.

- (4) On the UUT select Cal Points 1 to 20 (2023) or 1 to 40 (2024) in turn, adjusting the Cal Factor at each step until the reading displayed on the power meter is as close as possible to +19.00 dBm.

19 High power pulse system level

Test equipment

Description	Minimum specification	Example
Power meter	±0.1 dB from 30 kHz to 2.4 GHz	IFR 6960B with 6912 Sensor

Adjustment procedure

This adjustment sets up the overall RF frequency response in pulse modulation mode in 60 MHz steps. Cal Point 0 is at 30 MHz (the lowest specified point in pulse modulation mode), Cal Point 1 is at 60 MHz and the remaining cal points are in 60 MHz steps up to 1.2 GHz (2023) or 2.4 GHz (2024).

Notes

Instruments with software issues less than 1.06 are calibrated at +16 dBm.

For instruments fitted with Option 11, Cal Point 0 is at 10 MHz.

- (1) ZERO and AUTOCAL the power meter.
- (2) Connect the test equipment as shown in Fig. 3-6.
- (3) On the UUT select:

[MENU] 117 [ENTER]

The UUT will be set to +14 dBm at 30 MHz (10 MHz for instruments fitted with Option 11) Cal Point 0.

Adjust Cal Factor until the reading displayed on the power meter is as close as possible to +14.00 dBm.

- (4) On the UUT select Cal Points 1 to 20 (2023) or 1 to 40 (2024) in turn, adjusting the Cal Factor at each step until the reading displayed on the power meter is as close as possible to +14.00 dBm.

Adjustment procedure tables

For 2023 signal generator, serial number _____ / ____
 2024

- Option 1 no attenuator
 Option 2 DC operation
 Option 3 high power
 Option 4 high stability frequency standard
 Option 7 fast pulse modulation
 Option 10 1 V peak mod input
 Option 11 high power + fast pulse modulation

Modified password _____

Table 3-2 UTIL 102 Frequency standard adjustment

DAC	Value (0 to 255)
Coarse	_____
Fine	_____

Table 3-3 UTIL 103 Ext mod reference adjustment

DAC	Value (0 to 65535)
Ext mod ref	_____

Table 3-4 UTIL 104 Int mod offset adjustment

DAC	Value (-1000 to +1000)
Mod offset	_____

Table 3-5 UTIL 105 Int mod amplitude adjustment

DAC	Value (0 to 65535)
Mod amplitude	_____

Table 3-6 UTIL 106 FM factor adjustment

DAC	Value (0 to 65535)
FM factor	_____

Table 3-7 UTIL 107 Unlevelled mod adjustment

DAC	Value (0 to 65535)
Mod factor	_____

Table 3-8 UTIL 109 Levelled (ALC) mod adjustment

DAC	Value (0 to 255)
ALC DAC	_____

Table 3-9 UTIL 110 PM factor adjustment

DAC	Value (0 to 65535)
PM factor	_____

Table 3-10 UTIL 111 RF level adjustment

DAC	Value (0 to 255)
RF DAC A (6 dB atten)	_____
RF DAC B (18 dB atten)	_____

Table 3-11 UTIL 112 AM adjustment

DAC	Value (0 to 255)
DAC A (30%)	_____
DAC B (80%)	_____

Table 3-12 UTIL 113 AM flatness adjustment

ModF	DAC value (0 to 255)
3 kHz	_____
50 Hz	_____

Table 3-13 UTIL 114 RF level (normal system)

Cal point	Cal factor DAC value (-3600 to +3600)
0 (10 MHz)	_____
1 (120 MHz)	_____
2 (240 MHz)	_____
3 (360 MHz)	_____
4 (480 MHz)	_____
5 (600 MHz)	_____
6 (720 MHz)	_____
7 (840 MHz)	_____
8 (960 MHz)	_____
9 (1080 MHz)	_____
10 (1200 MHz)	_____
2024 ONLY	
11 (1320 MHz)	_____
12 (1440 MHz)	_____
13 (1560 MHz)	_____
14 (1680 MHz)	_____
15 (1800 MHz)	_____
16 (1920 MHz)	_____
17 (2040 MHz)	_____
18 (2160 MHz)	_____
19 (2280 MHz)	_____
20 (2400 MHz)	_____

Table 3-14 UTIL 115 Pulse system level

Cal point	Cal point (Option 7 or 11 fitted)	Cal factor DAC value (-3600 to +3600)
0 (30 MHz)	0 (10 MHz)	_____
	1 (60 MHz)	_____
1 (120 MHz)	2 (120 MHz)	_____
	3 (180 MHz)	_____
2 (240 MHz)	4 (240 MHz)	_____
	5 (300 MHz)	_____
3 (360 MHz)	6 (360 MHz)	_____
	7 (420 MHz)	_____
4 (480 MHz)	8 (480 MHz)	_____
	9 (540 MHz)	_____
5 (600 MHz)	10 (600 MHz)	_____
	11 (660 MHz)	_____
6 (720 MHz)	12 (720 MHz)	_____
	13 (780 MHz)	_____
7 (840 MHz)	14 (840 MHz)	_____
	15 (900 MHz)	_____
8 (960 MHz)	16 (960 MHz)	_____
	17 (1020 MHz)	_____
9 (1080 MHz)	18 (1080 MHz)	_____
	19 (1140 MHz)	_____
10 (1200 MHz)	20 (1200 MHz)	_____
	2024 ONLY	
11 (1320 MHz)	21 (1260 MHz)	_____
	22 (1320 MHz)	_____
12 (1440 MHz)	23 (1380 MHz)	_____
	24 (1440 MHz)	_____
13 (1560 MHz)	25 (1500 MHz)	_____
	26 (1560 MHz)	_____
14 (1680 MHz)	27 (1620 MHz)	_____
	28 (1680 MHz)	_____
15 (1800 MHz)	29 (1740 MHz)	_____
	30 (1800 MHz)	_____
16 (1920 MHz)	31 (1860 MHz)	_____
	32 (1920 MHz)	_____
17 (2040 MHz)	33 (1980 MHz)	_____
	34 (2040 MHz)	_____
18 (2160 MHz)	35 (2100 MHz)	_____
	36 (2160 MHz)	_____
19 (2280 MHz)	37 (2220 MHz)	_____
	38 (2280 MHz)	_____
20 (2400 MHz)	39 (2340 MHz)	_____
	40 (2400 MHz)	_____

Table 3-15 UTIL 118 Attenuator pads (not Option 1)

Cal point	33 dB	11 dB	33 dB	22 dB	33 dB
0 (10 MHz)	_____	_____	_____	_____	_____
1 (120 MHz)	_____	_____	_____	_____	_____
2 (240 MHz)	_____	_____	_____	_____	_____
3 (360 MHz)	_____	_____	_____	_____	_____
4 (480 MHz)	_____	_____	_____	_____	_____
5 (600 MHz)	_____	_____	_____	_____	_____
6 (720 MHz)	_____	_____	_____	_____	_____
7 (840 MHz)	_____	_____	_____	_____	_____
8 (960 MHz)	_____	_____	_____	_____	_____
9 (1080 MHz)	_____	_____	_____	_____	_____
10 (1200 MHz)	_____	_____	_____	_____	_____
2024 ONLY					
11 (1320 MHz)	_____	_____	_____	_____	_____
12 (1440 MHz)	_____	_____	_____	_____	_____
13 (1560 MHz)	_____	_____	_____	_____	_____
14 (1680 MHz)	_____	_____	_____	_____	_____
15 (1800 MHz)	_____	_____	_____	_____	_____
16 (1920 MHz)	_____	_____	_____	_____	_____
17 (2040 MHz)	_____	_____	_____	_____	_____
18 (2160 MHz)	_____	_____	_____	_____	_____
19 (2280 MHz)	_____	_____	_____	_____	_____
20 (2400 MHz)	_____	_____	_____	_____	_____

Option 3 or 11

Table 3-16 UTIL 116 High power RF level (normal system)

Cal point	Cal factor DAC value (-3600 to +3600)	2024 only cal points	Cal factor DAC value (-3600 to +3600)
0 (10 MHz)	_____	21 (1260 MHz)	_____
1 (60 MHz)	_____	22 (1320 MHz)	_____
2 (120 MHz)	_____	23 (1380 MHz)	_____
3 (180 MHz)	_____	24 (1440 MHz)	_____
4 (240 MHz)	_____	25 (1500 MHz)	_____
5 (300 MHz)	_____	26 (1560 MHz)	_____
6 (360 MHz)	_____	27 (1620 MHz)	_____
7 (420 MHz)	_____	28 (1680 MHz)	_____
8 (480 MHz)	_____	29 (1740 MHz)	_____
9 (540 MHz)	_____	30 (1800 MHz)	_____
10 (600 MHz)	_____	31 (1860 MHz)	_____
11 (660 MHz)	_____	32 (1920 MHz)	_____
12 (720 MHz)	_____	33 (1980 MHz)	_____
13 (780 MHz)	_____	34 (2040 MHz)	_____
14 (840 MHz)	_____	35 (2100 MHz)	_____
15 (900 MHz)	_____	36 (2160 MHz)	_____
16 (960 MHz)	_____	37 (2220 MHz)	_____
17 (1020 MHz)	_____	38 (2280 MHz)	_____
18 (1080 MHz)	_____	39 (2340 MHz)	_____
19 (1140 MHz)	_____	40 (2400 MHz)	_____
20 (1200 MHz)	_____		

Table 3-17 UTIL 117 High power pulse system level

Cal point	Cal factor DAC value (-3600 to +3600)	2024 only cal points	Cal factor DAC value (-3600 to +3600)
0 (30 MHz)	_____	21 (1260 MHz)	_____
1 (60 MHz)	_____	22 (1320 MHz)	_____
2 (120 MHz)	_____	23 (1380 MHz)	_____
3 (180 MHz)	_____	24 (1440 MHz)	_____
4 (240 MHz)	_____	25 (1500 MHz)	_____
5 (300 MHz)	_____	26 (1560 MHz)	_____
6 (360 MHz)	_____	27 (1620 MHz)	_____
7 (420 MHz)	_____	28 (1680 MHz)	_____
8 (480 MHz)	_____	29 (1740 MHz)	_____
9 (540 MHz)	_____	30 (1800 MHz)	_____
10 (600 MHz)	_____	31 (1860 MHz)	_____
11 (660 MHz)	_____	32 (1920 MHz)	_____
12 (720 MHz)	_____	33 (1980 MHz)	_____
13 (780 MHz)	_____	34 (2040 MHz)	_____
14 (840 MHz)	_____	35 (2100 MHz)	_____
15 (900 MHz)	_____	36 (2160 MHz)	_____
16 (960 MHz)	_____	37 (2220 MHz)	_____
17 (1020 MHz)	_____	38 (2280 MHz)	_____
18 (1080 MHz)	_____	39 (2340 MHz)	_____
19 (1140 MHz)	_____	40 (2400 MHz)	_____
20 (1200 MHz)	_____		

Chapter 4

INITIAL REPAIR

The following describes the action that should be taken if the instrument appears to be dead, either following delivery or during the normal course of operation. The only test equipment that is required is a suitable screwdriver and a digital voltmeter.

- (1) For an instrument fitted with Option 2 and the AC operation is functioning correctly, check the DC supply, the supply cable and the rear panel DC fuse.
- (2) Check the AC supply, the supply cable and the rear panel AC fuse.
- (3) Remove the instrument cover and check the internal supplies as follows:

AC power supply

- (1) Check the 2 A fuse.
- (2) Check the following DC outputs:-

V1	Orange	+5 V
V2	Red	+12 V
V3	Yellow	+24 V
V4	Grey	-12 V

AC/DC power supply

- (1) Check connector A:-

Pin 1	0 V
Pin 2	Polarising key
Pin 3	-12 V
Pin 4	+5 V
Pin 5	+12 V
Pin 6	Battery V
Pin 7	Not used

- (2) Check connector B:-

Pin 1	0 V
Pin 2	-12 V
Pin 3	Polarising key
Pin 4	+5 V
Pin 5	+12 V
Pin 6	Not used
Pin 7	+24 V

- (3) Check connector C:-

Pin 1	+12 V
Pin 2	0 V
Pin 3	Polarising key

Chapter 5

FAULT DIAGNOSIS

Contents

Introduction	5-2
Latch access	5-2
General guide to fault finding.....	5-2
Instrument dead	5-2
RF level and AM faults	5-2
FM and Φ M faults	5-3
DSP source and FM routing checks.....	5-4
FM D-A converter and FM attenuator checks	5-4
Pulse modulation faults	5-5
Error message guide to fault finding.....	5-5
1 EEPROM checksum.....	5-5
2 Pad cal checksum.....	5-5
3 RF cal checksum	5-5
4 Freq. std checksum.....	5-5
5 Synthesizer cal checksum	5-5
6 Mod ref. checksum	5-5
7 Mod offset checksum.....	5-6
8 Mod amp checksum.....	5-6
9 ALC cal checksum	5-6
10 FM cal factor checksum.....	5-6
11 FM tracking checksum	5-6
12 FM cal factor checksum.....	5-6
13 System cal checksum	5-6
14 AM cal checksum.....	5-6
15 Store checksum	5-6
16 Image checksum.....	5-6
20 Frac N out of lock at <freq>.....	5-6
21 VCO cal fail at <freq>.....	5-6
22 VTF tune cal fail at <freq>	5-6
23 FM tracking cal fail at <freq>.....	5-6
500 RPP tripped	5-7
501,502 Fractional-N loop low, Fractional-N loop high.....	5-7
503 Ext. standard missing	5-9
504 Ext. standard frequency low 505 Ext. standard frequency high	5-10
506 VCXO loop low.....	5-10
507 VCXO loop high	5-10
508 Amplitude mod unlevelled.....	5-11
509 Output unlevelled	5-11
510 High power amplifier failed	5-12
511 ALC too high 512 ALC too low	5-13
513 DSP not responding	5-13
(549 RF level uncalibrated).....	5-13
590 Main RAM faulty	5-13
591 Main PROM faulty	5-13

Introduction

This fault finding guide is aimed at technically competent service engineers. The guide will narrow down the search for any fault to a circuit area but not down to a component level. It is split into two sections, the first deals with faults that may not result in an error message being reported by the instrument and the second which deals with faults that the instrument will report with an error message on the screen. The UTILS screen showing the full complement of reported errors should be checked before proceeding with any fault finding exercise to determine where the fault is most likely to lie.

Latch access

A facility for controlling the instrument DACs and latches is available under the diagnostic menu. Latches are numbered from 0 to 255. These latches are very helpful in diagnosing instrument faults.

General guide to fault finding

Instrument dead

There are some faults which may occur which would prevent any error messages being displayed.

Screen blank and unlit

Carry out the following:

- (1) Check the input fuse in the mains inlet socket on the back of the instrument and in the mains cable plug.
- (2) Check the primary cables and mains switch and ensure that they are all connected correctly.
- (3) Check the PSU DC outputs to see if they are at the correct level.
- (4) Check that the cables to the front panel are all fitted correctly.

Additional information

The fuse fitted in the mains inlet socket is a 2A-T, 20 mm x 5 mm cartridge type.

If none of the above work then proceed onto the list below.

Screen blank and lit

Using the control board AB1 circuit diagrams proceed as follows:

- (1) Check the reset line on IC206; if the instrument is being held in reset it could be because the DC supplies are faulty.
- (2) Check the DC levels of the power supply lines.
- (3) The software could be getting stuck in a loop; this could be due to faulty EEPROM, SRAM or peripheral part of the instrument that requires initialisation, i.e. the frequency standard or audio generator DSP (see fault finding guide for these sections further on in the document).

RF level and AM faults

Using the control board AB1 circuit diagrams proceed as follows:

- (1) Trace the modulation signal, internal or external, through from AM source selection multiplexer IC22 to the output of IC24 (b). DAC IC25 is used to apply the depth of modulation information onto the modulating signal.
- (2) Trace the signal from IC24 (b) through to the output of IC24 (d). This takes the modulating signal and applies square law correction to it and finally amplifies it to an appropriate level for use in the RF tray as the AM modulating signal.

- (3) Trace the signal from IC24 (b) through to the output of IC26 (d). IC27 in this path is used to apply the RF level information onto the modulating signal. This is before square law correction and amplification is applied to it for use in the RF tray as the RF level signal.
- (4) Go to paragraphs covering errors 508 and 509 for the AM and RF level faults on RF board AA1.

Useful latches for AM and RF level diagnosis

The depth of modulation DAC can be adjusted using latches 62 & 63 in 16-bit mode.

The RF level DAC can be adjusted using latches 66 & 67 in 16-bit mode.

The AM square law correction can be adjusted using latch 65.

The AM offset can be adjusted using latch 64.

The RF level square law correction can be adjusted using latch 69.

The RF offset can be adjusted using latch 68.

Latch 71 can be used to determine which of the inputs is used. This enables the internal 1 Vcal signal to be selected if required.

FM and Φ M faults

The internal modulating signal is produced by the digital signal processor on the control board. Either the internal or external modulation source is selected by a multiplexer and the signal is routed to the RF board. On the RF board the signal feeds two paths. The signal is digitised using a one-bit A-D converter and the resulting bit stream is used to directly modulate the synthesiser. It can provide FM with modulation rates from DC to 3 kHz. The signal is also scaled using a multiplying DAC and switched attenuators. This signal modulates the VCO to provide FM with modulation rates from 3 kHz to 100 kHz.

The following tests can be performed without removing the covers:

- (1) Set FM internal, deviation of 10 kHz and mod rate of 100 Hz. Enable modulation and mod source. Using an oscilloscope check to see that there is a 2 V RMS sine wave of 100 Hz at the LF OUTPUT socket. This verifies the internal source is working. If no signal is present, check the DSP audio generator on the control board (Sheet 2).
- (2) Set FM internal, deviation of 10 kHz and mod rate of 100 Hz. Connect a modulation analyser to the output and observe that the correct deviation and mod rate is produced. This verifies that the internal modulation source routing and the one-bit A-D converter is working. If a fault is found look at FM routing and the FM A-D converter.
- (3) Set FM external, DC coupled and deviation of 10 kHz. Enable modulation and mod source. Perform DC FM nulling. Connect a frequency counter to the RF output. Apply 1 V DC to the EXT MOD INPUT socket. A shift of 7.07 kHz should be observed in the output frequency. This verifies that the one-bit A-D converter and external FM path is working. If a fault is found look at FM routing and the FM A-D converter.
- (4) Set FM external, AC coupled and deviation of 10 kHz. Enable modulation and mod source. Apply a 50 kHz, 1 V RMS sinewave to the EXT MOD INPUT socket. Connect a modulation analyser to the output and observe that the correct deviation is produced. If a fault is found check the FM attenuator and drive sections on the RF board (Sheet 5).
- (5) Set FM external, ALC coupled and deviation of 10 kHz. Enable modulation and mod source. Apply a 1 kHz, 1 V RMS sinewave to the EXT MOD INPUT socket. Connect a modulation analyser to the output and observe that the correct deviation is produced. Apply a 1 kHz, 1.5 V RMS sinewave to the EXT MOD INPUT socket and check that the measured deviation does not change. If either test fails then the automatic level control circuit is faulty. Refer to the 'Error messages' section and '511 ALC too high, 512 ALC too low' for more diagnostic information.

- (6) Phase modulation will not work if frequency modulation is not working. If phase modulation is not working but frequency modulation is, then the differentiator section or switch is faulty. Refer to FM routing checks for more diagnostic information.

DSP source and FM routing checks

Using the control board AB1 circuit diagrams proceed as follows:

- (1) Before removing the covers, enable the modulation and turn it on. Measure the output from the LF OUTPUT socket on the front panel - the signal should be 2 V RMS from a 600 Ω source impedance. The frequency should be whatever is set as the modulation frequency on the front panel. If this signal is present, carry on with the next stage, if not, check the output of filter chip IC14 to see if the signal is present there. If it is not, trace the signal route back to serial DAC IC13, and to the DSP itself. Also refer to the 'Error messages' section and '513 DSP not responding' for more diagnostic information.
- (2) Trace the modulation signal, internal or external, through from FM source selection multiplexer IC32 to the output of IC49 (b). If FM is selected switch IC29 (b) will be using the 2Y1 input, pin 1, and if Φ M is selected switch IC29 (b) will be using the 2Y0 input, pin 2. In FM mode the signal is amplified slightly and remains at a constant level across the input frequency range. In Φ M mode the signal is differentiated causing the signal level to vary across the input frequency range at a rate of 6 dB/octave; at 10 kHz the level should be nominally 1 V pk.

Latch access:

Latch 71 can be used to determine which of the inputs is used for the FM source multiplexer. This enables the internal 1 Vcal signal or 0 V to be selected if required.

FM D-A converter and FM attenuator checks

Using the RF board AA1 circuit diagrams proceed as follows:

- (1) Set FM internal, 1 kHz mod rate and 100 kHz deviation. Enable modulation and mod source. Referring to Sheet 3, ensure that a 1 kHz tone with an amplitude of 1 V pk is present on the input of R352. If not, check the cable between the control board and the RF board.
- (2) Check that IC304(a) pin 4 is not stuck at 0 V. Check that a 5 MHz CMOS compatible clock is present at pin 3. A pseudo random bit-stream should be present at TP10 if the converter is operating.
- (3) Check that -5 V is present on IC301 pin 1 and that +5 V is present on IC304 pin 14. The voltage on TP11 is derived from gate array IC305 and is used to null out voltage offsets. Under normal operating conditions the voltage at TP11 should be close to 1.25 V.
- (4) Check loop integrators IC301(b), (c), (d) and inverter stage TR301 and IC304(a) for correct function.
- (5) Referring to Sheet 5, check that a 1 kHz sine wave with an amplitude of 1 V is present on pin 15 of IC409. Check that a 1 kHz signal is present on pin 7 of IC405(b). The level of this signal is controlled by the data word written to IC409. The word can be accessed using latches 53 and 54 in 16-bit mode. With a full scale of 4095 written to the DAC there should be a 1 V RMS signal on pin 7 of IC405(b).
- (6) Check to ensure that a 1 kHz signal is present on pin 1 of IC405(a). The level of this signal will depend on the setting of the FM attenuator. The attenuator can be controlled using bit 0 and bit 1 of latch 1. Attenuation can be set to 0, 20, or 40 dB or the signal path grounded. The second attenuator stage uses a relay switch and is controlled by bit 2 of latch 1. This has an attenuation of 0 or 40 dB.

Pulse modulation faults

There are one of two different types of pulse modulator fitted in the instrument. Instruments fitted with a slow pin-diode pulse modulator (boards AA2 or AA2/1) have a PULSE I/P socket on the rear panel. The optional fast pulse modulator, based on FET switches and fitted to Option 7 (board AA2/5) and Option 11 (board AA2/7) instruments, has a PULSE INPUT socket on the front panel. The following provides brief diagnostic information for these two modulators:

Standard modulator

Using board AA2 or AA2/1 circuit diagrams proceed as follows:

Before removing the instrument covers check that relays RLA and RLB are switching, by enabling and disabling the modulator via the utility menu UTIL 22 and listening for the relay clicking sound. If the relays appear not to be switching, suspect the drive circuitry located on RF board AA1. Measure the PULSE I/P socket impedance, which should be around 10 k Ω . If short or an open circuit, trace it back to the source of the fault after removing the instrument covers. Suspect diodes D1 to D7 if the modulator RF on/off ratio is not correct or if the insertion loss is more than 5 dB. Also check for open circuits due to faulty capacitors C1 to C4.

Fast pulse modulator

Using board AA2/5 or AA2/7 circuit diagrams proceed as follows:

Before removing the instrument covers check that relays RLA and RLB are switching, by enabling and disabling the modulator via the utility menu UTIL 22 and listening for the relay clicking sound. If the relays appear not to be switching, suspect the drive circuitry located on RF board AA1. Measure the PULSE INPUT socket impedance, which should be between 45 and 55 Ω . If short or an open circuit, trace it back to the source of the fault after removing the instrument covers. Also check that the pulse input signal applied to the PULSE INPUT socket reaches the modulator by tracing its path.

If the pulse modulator does not appear to translate +5 V and 0 V, at pulse input, to RF on/off, check that the +5 V and -5 V supplies are present on pins 3 and 5 of IC8/9 respectively, and that these voltages also appear on pins 1 and 8 of IC8/9. When logic transition occurs at the PULSE INPUT socket the voltages on pins 1 and 8 of IC8/9 should exchange values. Other low RF level problems are most likely due to faulty FET switches (ICs 4 to 7) or FET amplifier TR4 failures.

Error message guide to fault finding

The following is a list of the relevant errors, in numerical order, that may be reported by the instrument to indicate a fault condition:

1 EEPROM checksum

The checksum stored in the main EEPROM on the control board does not match the checksum calculated by the processor when it checked the stores on power-up. This probably means that EEPROM IC7 on control board AB1 needs to be replaced. If this is done, the instrument serial number will have to be re-entered using the super-user password and a full recalibration will have to be performed.

2 Pad cal checksum

3 RF cal checksum

4 Freq. std checksum

5 Synthesizer cal checksum

6 Mod ref. checksum

- 7 Mod offset checksum**
- 8 Mod amp checksum**
- 9 ALC cal checksum**
- 10 FM cal factor checksum**
- 11 FM tracking checksum**
- 12 FM cal factor checksum**
- 13 System cal checksum**
- 14 AM cal checksum**
- 15 Store checksum**
- 16 Image checksum**

None of the error messages from 2 to 16 should ever be seen by the user. These error messages were used for diagnostics when debugging the software. If one of these checksums were to be in error the appropriate EEPROM checksum error message would be seen on the screen instead.

20 Frac N out of lock at <freq>

The synthesiser calibration routine attempts to find optimum pre-steer values for the VTF and VCO at 50 MHz intervals from 1200 MHz. This error indicates that the auto-calibration routine could not achieve phase lock of the synthesiser during the auto-calibration. For diagnostic information refer to error '501,502 Fractional-N loop low, Fractional-N loop high'.

21 VCO cal fail at <freq>

This error indicates that the synthesiser auto-calibration routine could not find the optimum pre-steer value. This probably indicates that auto-cal comparator IC406(b) is faulty or the cal disable line is stuck at 5 V.

22 VTF tune cal fail at <freq>

The synthesiser calibration routine attempts to find optimum pre-steer values for the VTF and VCO at 50 MHz intervals from 1200 MHz. This error indicates that the auto-calibration routine could not find the optimum pre-steer value for setting the voltage tuned filters. The routine attempts to locate the peak of the filter response by monitoring the control voltage of the AM levelling loop. Check the AM levelling loop (Sheet 6) or the level readback comparator IC501(a). For more diagnostic information refer to 'Error 508 Amplitude mod unlevelled'. If the AM levelling loop appears to be functioning there may be a problem with low signal level from the VTF. In this case refer to '501,502 Fractional-N loop low, Fractional-N loop high'.

23 FM tracking cal fail at <freq>

The synthesiser calibration routine attempts to match the FM deviation produced by modulating the synthesiser with the deviation produced by modulating the VCO. It does this by adjusting FM control DAC IC409 (Sheet 5). The calibration is performed in 25 MHz steps starting at 1200 MHz. This error indicates that the auto-calibration routine could not match the sensitivity of the two FM paths. This could be due to a fault with the FM auto-cal circuit, IC407 (Sheet 4), or a fault with the FM path or FM source. For more diagnostic information refer to section 'FM and Φ M' above.

500 RPP tripped

Using the AA2, AA2/1, AA2/5 and AA2/7 boards' circuit diagrams proceed as follows:

The Reverse Power Protection (RPP) facility protects the instrument from damage level signals present on the RF OUTPUT socket. This error message may be due to an externally applied offending signal on the output port which can be checked easily by disconnecting anything connected to the output port and terminating it with a 50 Ω load. If the error message remains it must be due to a number of hardware faults within the instrument. In order to locate the fault go through the following check list:

- (1) If the RPP can not be reset even after terminating the output with 50 Ω , try switching the instrument OFF and ON again. If the fault goes away measure RPP tripping levels by applying an external DC voltage to the RF OUTPUT socket. The RPP should trip around 4 V for the standard attenuator and 11 V for a high power option. If, however, it is still not resettable the instrument must be opened-up to locate and fix the fault. If, however, the instrument does reset continue this sequence.
- (2) RPP trips when switching into or out of the BFO frequency band (9 kHz to 10 MHz) but is resettable. The most likely cause is a large difference in RF level between the straight through and the BFO band paths, possibly due to a broken capacitor in the path or amplifier failure resulting in different levels.
- (3) If the instrument has a high power option fitted and the RPP only trips above +7 dBm suspect the high power amplifier section (go to error '510 High power amplifier failed').
- (4) If the RPP tripping point is frequency or level dependent above 10 MHz or the relay keeps tripping when trying to reset, the most likely cause is a broken RPP reed-relay (RLM) or the output RF level is much higher than set. Check relay (RLM) and RF level output.
- (5) Another cause of RPP tripping could be a large DC voltage on the RF output line due to the breakdown of capacitor C845 on the RF board AA1. Measure the DC voltage level on the RF output line. If greater than 0.1 V change capacitor C845 and remeasure the DC voltage level.

501,502 Fractional-N loop low, Fractional-N loop high.

These error messages can be caused by a number of faults on RF board AA1.

Note

The 2023 synthesiser section is identical to the 2024 synthesiser, and generates an octave from 1.2 to 2.4 GHz. However, a 2023 is limited to 1.2 GHz output. When repairing a 2023 synthesiser entering exactly half the frequency specified in the following section will have an identical effect. For instance instead of setting a frequency of 1201 MHz, set a frequency of 600.5 MHz for a 2023.

The following tests can be performed without removing the covers:

- (1) Step the carrier frequency from 1201 MHz to 2400 MHz in 100 MHz steps and note the frequencies at which the error is displayed. If the error is not present at some of the frequencies it indicates correct operation of main dividers IC307 and IC309, controller IC305, phase detector IC310, 311 and 312, and loop filter and lock detector IC402, IC404 and IC406. If the error appears at all frequencies refer to the 'General synthesiser fault diagnosis' section below.
- (2) The VCO and filter are controlled by pre-steer voltages. If the pre-steer is not correct this will produce lock errors. The VCO pre-steer DAC value must be within ± 3 of the nominal value for correct lock to occur. The VTF pre-steer DAC value can be as much as ± 15 from the nominal value before lock errors will occur. The VCO pre-steer DAC (Latch 2) and VTF pre-steer DAC (Latch 3) can be modified using the latch access facility to identify faults caused by incorrect pre-steer values.
- (3) Pre-steer values are derived by an automatic calibration routine (Cal routine 100). If pre-steer problems are suspected, running this routine will cure the problem if no other hardware problems exist. If the routine cannot complete the calibration due to a hardware malfunction an error message is displayed to help identify the problem.

- (4) The top synthesised octave is generated in three ranges. The VTF tunes continuously from 1.2 to 2.4 GHz whilst the VCO is tuned in the three bands shown below:

Synthesiser frequency	VCO frequency
1201 - 1600 MHz	400 - 533 MHz
1601 - 2000 MHz	400 - 500 MHz
2001 - 2400 MHz	400 - 480 MHz

- (a) If a lock error is found to repeat through the bands it is likely that the VCO or harmonic generator is faulty. For example an error at 1201 MHz, 1601 MHz and 2001 MHz would suggest a fault with the VCO at the bottom of its tuning range. Refer to 'VCO and harmonic generator diagnosis' below.
- (b) A fault between 1500 MHz and 1600 MHz only will indicate a problem with the VCO at the top of the band. This could be caused by a pre-steer fault limiting the maximum tuning range, or by a problem with the VCO itself. Refer to 'VCO and harmonic generator diagnosis' below.
- (c) A fault appearing only at the top or bottom of the 1.2 to 2.4 GHz range suggests a problem with the VTF. For example, a fault between 1.2 to 1.3 GHz only or a fault between 2.2 to 2.4 GHz only. Refer to 'VTF fault diagnosis' below.

The following tests will require access to the RF board.

General synthesiser fault diagnosis

- Check that the voltage on TP14 is outside the range ± 8 V. If not, check the operation of lock window comparator IC406(c),(d).
- Check that 25 MHz is present on IC205 pin 9 and that 5 MHz is present on pin 3 of IC313. If not, refer to error '506 VCXO loop low' or '507 VCXO loop high' to debug the reference loop.
- Using an oscilloscope examine the signal on TP7. A pulsed signal should be present with an amplitude of 5 V and a pulse width of 25 to 50 ns. If no signal is present check IC307, IC310 and the correct bias of TR302, TR303.
- Using a frequency counter measure the frequency of the signal on TP7. If the signal has a frequency close to 5 MHz (± 50 kHz), it is likely that the fault is within the phase detector or loop filter components. If the phase detector is operating, the voltage on pin 3 of IC402 should be at 5 V if the signal is above 5 MHz, or at 0 V if the signal is below 5 MHz. If this is correct, examine loop filter components IC402 and IC404 for correct operation.
- If the frequency on TP7 is a long way from 5 MHz the control ASIC is not setting the correct divide ratio or IC307 does not have a suitable signal input. Check that the DC bias on the input of IC308 is approximately 1.5 V, and 4.5 V on the output. Check that the bias on TR305 collector is approximately 5 V. Set the carrier frequency to 1.4 GHz. Check to see if a signal at 1.4 GHz is present at C339 input with a level in the range -5 dBm to $+2$ dBm. If the signal is off frequency or at a low level, adjust latch 2 and latch 3 using the latch poke facility. If a signal with the correct power and frequency cannot be obtained refer to 'VCO and harmonic generator diagnosis' and 'VTF fault diagnosis' below. Check to see whether a 700 MHz signal is present at the output of IC309 and at the input of IC307.
- The divide control word can be monitored on the pins of IC307. The table below gives the voltages that should appear for the two different carrier frequencies.

IC307 pin no.	Set carrier 1.32 GHz	Set carrier 2.36 GHz
27 (MSB)	2.5 V	2.5 V
28	0 V	2.5 V
1	0 V	2.5 V
2	0 V	0 V
3	0 V	2.5 V
16	Toggling	Toggling
15	Toggling	Toggling
14 (LSB)	Toggling	Toggling

If no pins are toggling check TP8 to see whether the ASIC clock is present. The ASIC power supply can be checked on pin 25 of the 25-way D-connector. Check that pin 50 of IC305 (panic) is not permanently high. Check the control interface to IC305.

VCO and harmonic generator diagnosis

Proceed as follows:

- (1) Remove the cover of the 400 to 533 MHz VCO. Connect a spectrum analyser to the output end of R107. Using the latch access facility set latch 2 to a value of 40. Check that a signal is present with a frequency of 380 to 400 MHz. If no signal is present check bias of TR101. Using the front panel knob tune the latch value from 40 to 220 and check that the frequency can be tuned from 400 to 533 MHz. If the frequency cannot be correctly tuned check VCO pre-steer circuit (Sheet 4), IC401 and associated components. Check correct connection of oscillator varactor diodes D101 to D106.
- (2) Set VCO frequency to 400 MHz using the latch access facility. Disconnect the spectrum analyser from the VCO. Check that DC bias of IC101 input is about 1.5 V and output is 4.5V. Check that bias of TR102 collector is about 6 V. Adjust trimmer capacitor C114 for a maximum DC voltage on TP15. The peak voltage should be 0.5 to 1 V. If the voltage is significantly less, check TR102 collector tuning components and D107.

VTF fault diagnosis

Proceed as follows:

- (1) Check the bias to amplifiers IC104, IC105, IC106 and IC107 within the filter section. The amplifiers should have a nominal voltage at the input pin of 1.5 V and a voltage at the output of 4.5 V.
- (2) Probe the tuning voltage on C156. Using the latch access utility adjust the value of latch 3 between 0 and 255 and make sure that the voltage varies between 0 and 23 V. If not, check IC102 and IC103.
- (3) Probing on the centre point of each pair of varactor diodes D108 to D123, check that the correct tune voltage is present.
- (4) Set the VCO to 400 MHz using latch 2 and the VTF to 1.2 GHz by setting latch 3 to a value of 48. Check signal levels throughout the filter. Amplifiers should give 10 to 12 dB gain and the single filter section loss should be approximately 8 dB.

503 Ext. standard missing

Using the control board AB1 circuit diagrams proceed as follows:

- (1) Check that the external standard is present and connected to the correct rear panel connector.
- (2) Trace the standard signal through the input conditioning circuitry, from C13 to IC63(d).

- (3) Check out the frequency detector circuitry, from IC41(a) to IC63(f).
- (4) If all this looks correct, check the interrupt handler through to the output of IC24(b). Another way to check the interrupt handler is to see if the other interrupts are being reported correctly, i.e. ALC LOW, etc.

504 Ext. standard frequency low**505 Ext. standard frequency high**

Using the control board AB1 circuit diagrams proceed as follows:

- (1) Check that the external frequency standard is either 1 MHz \pm 3 Hz or 10 MHz \pm 30 Hz and that the measured frequency corresponds to the selected frequency on the UTILS frequency standard screen.
- (2) Check that multiplexer IC36 is set to the correct settings. If the TCXO detect circuitry is faulty, switch 2 on the multiplexer could be switched to the incorrect input.
- (3) Check the frequency limits window comparator for correct operation, the window comparator is based round IC43(c) & (d) - the window limits are marked on the circuit diagram.
- (4) Check the operation of the phase-locked-loop (PLL) circuit, this is based round IC44, IC40 and IC43(a), and operates at 1 MHz input frequency.
- (5) Check the frequency of the internal frequency standard whilst the instrument is set to run from the internal frequency standard. If this frequency is too far away from the nominal 10 MHz, there might not be enough tuning range for the PLL to compensate for.

Latch access

Latch numbers 112 & 113 in 16-bit mode can be used to determine the tuning range of the internal frequency standard. These latches control the oscillator tune voltage from DAC IC34(f),(g), and can be set to give from -3 V to +3 V on their outputs.

506 VCXO loop low

Refer to board AA1, Sheet 2 and proceed as follows:

- (1) Check voltage on IC204 pin1. If this is greater than 1 V check lock comparator IC204(d).
- (2) Check TP2 to ensure a 10 MHz \pm 100 Hz squarewave is present with an amplitude greater than 3.5 V. If not, check the cable connecting the 10 MHz standard from the control board.
- (3) Check that the supply voltage to the phase detector and dividers is greater than 4 V. Check that supply IC204 pin 4 is greater than +22 V.
- (4) Check TP3 to ensure a squarewave is present with a frequency close to 10 MHz. If not, check IC202 for divide by 5 and IC205a for divide by 2 operation.
- (5) If the frequency of the squarewave on TP3 is greater than that on TP2, check VCXO tuning components. Otherwise, check voltage on IC204 pin 12. If this is below 2.5 V, check phase detector IC201 and IC203. If the voltage is above 2.5 V, check loop filter IC204(a),(b) and associated components.

507 VCXO loop high

Refer to board AA1, Sheet 2 and proceed as follows:

- (1) Check the voltage on IC204 pin1. If this is less than 19 V, check lock comparator IC204(d).
- (2) Check that the -11 V supply is present on L205.
- (3) Check for a 100 MHz signal on TR202 collector with a pk-pk amplitude of approximately 1 V. If this is not present, check that the bias of TR201 and TR202 is correct. Check the crystal and associated tuning components. If no fault is found, adjust C215 to produce a maximum amplitude signal at TR202 collector. The signal should be a few kHz higher than 100 MHz.

- (4) Check TR205 collector for a signal of approx. 4 V pk-pk at 100 MHz.
- (5) Check IC205 pin 6 for a 50 MHz squarewave with an amplitude greater than 3.5 V. Check TP3 for a 10 MHz squarewave.
- (6) Check TP2 to ensure that a 10 MHz \pm 100 Hz squarewave is present with an amplitude greater than 3.5 V. If not, check cable connecting the 10 MHz standard from the control board.
- (7) Check the voltage on IC204 pin 12. If this is greater than 2.5 V, check phase detector IC201, IC203. Otherwise check loop filter IC204(a),(b) and associated components.

508 Amplitude mod unlevelled

The amplitude modulator is responsible for applying AM to the carrier. To do this a voltage-controlled pin diode modulator and envelope detector are used in a controlled loop to apply AM to the carrier. The modulator control voltage comes from control board AB1.

Using RF board AA1 circuit diagrams proceed as follows:

- (1) If the error only appears at some frequencies and levels and not at others, the most likely cause is insufficient RF level present at the input of the modulator. When this occurs, the AM distortion and AM accuracy will get worse with the loop running out of the levelling range. One of the main reasons for insufficient RF input level is most likely to be a failure of band-pass filters which divide the frequency from 1.2 to 2.4 GHz all the way down to 10 MHz. The following table lists the changeover frequencies for each filter:

No.	Carrier frequency range	Filter type selected
1	10 kHz to 10 MHz	BFO band
2	>10 MHz to 18.75 MHz	18.75 MHz LPF
3	>18.75 MHz to 37.5 MHz	37.5 MHz LPF
4	>37.5 MHz to 75 MHz	75 MHz LPF
5	>75 MHz to 150 MHz	150 MHz LPF
6	>150 MHz to 300 MHz	300 MHz LPF
7	>300 MHz to 420 MHz	420 MHz LPF
8	>420 MHz to 600 MHz	600 MHz LPF
9	>600 MHz to 1200 MHz	1200 MHz LPF
10	>1200 MHz to 2400 MHz	Through band

- (2) If the error only occurs within one filter band frequency, it is most likely that the problem lies with that filter.
- (3) If the error is present at all frequencies, either detector D510 is damaged or other AM related circuitry is malfunctioning.

509 Output unlevelled

Using RF board AA1 circuit diagrams proceed as follows:

The fine RF output level control range is obtained using an Automatic Level Control (ALC) loop which consists of level modulator D512/D513 followed by RF power amplifiers TR806 to TR808 and TR814 and an RF level detector D804 at the end. The detector output is compared with the corresponding RF level DAC output from control board AB1 by comparator IC802(c).

Comparator output is used to adjust the level. When the adjustment range on the level modulator runs out, *Err 509: Output unlevelled* appears on the screen. There can be a number of causes which result in this error being generated. The main reasons are covered in the following points:

- (a) **Incorrect calibration** - Set RF level to +7 dBm and measure the output level at a frequency where an error is being displayed. If the level is out by more than 1 dB then try the RF levels calibration (UTIL_114). If the instrument can not be calibrated and/or the error is still displayed, it is not a calibration problem. Continue this sequence.
- (b) **Insufficient gain** - Output unlevelled errors which appear only at certain frequencies and RF levels, especially near the maximum output level, are most likely caused by failure of one or more amplifying stages, resulting in insufficient gain within the ALC loop. Check DC bias conditions on TR806 to TR808 and TR814 (see table below) as well as feedback and coupling capacitors.
- (c) **BFO failure** - Carrier frequencies below 10 MHz are generated by mixing a fixed 100 MHz VCXO with 100 to 110 MHz carrier and low-pass filtering the difference product. This method of obtaining low frequencies is performed using a Beat Frequency Oscillator (BFO). Therefore if the output unlevelled error only occurs below 10 MHz, the fault is most likely to be in the BFO section. Transistors TR815 to TR820 are configured as a double balanced Gilbert cell mixer with TR823 and TR824 configured as constant current sources. Transistors TR812, TR821 and TR822 are buffer amplifiers. Check that BFO TR810, TR811 is switching properly and that all the transistors are biased correctly.
- (d) **Failure of the levelling detector resulting in low detected voltage.** - One symptom of this will be large error in the output RF level. Set the carrier frequency to 1 GHz and adjust the output RF level to +10 dBm and then measure the voltage across detector diode D804. If the voltage is outside the range 0.6 to 1.0 V, the detector is most likely to be damaged; also check other components around the detector diode.

If *Err: 508 Amplitude mod unlevelled* is also displayed, the most likely reason is insufficient RF level going into the level modulator. The input level should be around -2 dBm.

- (e) **Levelling modulator faulty** - Check D512, D513 and TR508 biasing conditions (see table below).

Check comparator IC501(b).

Board	Component ref	Collector voltage
AA1	TR506	7.6 V
AA1	TR508	7.6 V
AA1	TR510	9.0 V
AA1	TR806	9.0 V
AA1	TR807	7.6 V
AA1	TR808	16.4 V
AA1	TR812	7.8 V
AA1	TR814	7.0 V
AA2/1	TR1	16 V
AA2/1	TR2	16 V

Note: Collector voltages will normally vary upto 10%.

510 High power amplifier failed

Using high power amplifier board AA2/1 or AA2/7 circuit diagrams proceed as follows:

- (1) The high power amplifier is switched by two relays (RLN & RLP) and is only enabled for levels above +7 dBm at all frequencies. Make sure that the RF output is terminated with 50 Ω. Toggle the RF level between +7 dBm and +8 dBm, using the up and down keys, and listen for the relay clicking sound. If relays appear not to be switching, suspect the drive circuitry for amplifier relay switching on the RF board AA1. If the relays are switching and the RF level above +7 dBm is within the specification, either the high power detector is not calibrated or it is faulty. Unlock the instrument to level two then enter the level calibration

utility (UTIL: 116 High Power System) and sequence through the 40 calibration points without changing the corresponding cal values. Save the cal data then exit the calibration routine. If the error still persists, check the DAC values.

- (2) If there is large error in the RF output level, suspect the high power amplifier section. Check the biasing of transistors TR1 and TR2. The collector voltages on both transistors should be around +16 V and the collector currents around 100 mA and 300 mA respectively. Also check that the feedback components are not broken.

511 ALC too high

512 ALC too low

Using the control board AB1 circuit diagrams proceed as follows:

- (1) Check that the modulation input signal is present and that the level is within the range that can be levelled by the ALC loop. This is given as being between 0.75 V RMS and 1.25 V RMS although the actual levelling range will be greater.
- (2) Trace the signal through the input conditioning circuitry, RLA to IC30 (a). At the output of IC30(a) the signal level should be about 73% of the input level.
- (3) Check the output level of IC48. This should be 1 V pk if it is calibrated. If it is not calibrated, it should still be fairly close to 1 V pk.
- (4) Check window comparator IC47(a),(b) for correct operation.
- (5) Check the positive and negative peak detectors, D12 to IC30(b), and the peak level filter, C26 to IC30(c). These provide the voltage feedback which controls variable resistor TR6 and hence the gain of levelling op-amp IC48.

Latch access

Latch number 70 can be used to adjust the output level of the ALC circuit; the adjustment range is about \pm a few mV from the mid-point setting.

513 DSP not responding

Using the control board AB1 circuit diagrams proceed as follows:

- (1) Ensure that there is a 10 MHz clock signal present at DSP IC12. If there is no clock, the DSP will not run at all.
- (2) Check the DSP bridge circuitry based around IC10, IC11, IC50(b) and IC51(b). This enables the DSP software to be downloaded by DMA from the microprocessor and then provides the normal DSP bridge signals when in normal operation.

(549 RF level uncalibrated)

This error message only appears where an RF level is set that the instrument specification does not support, even though the software allows the level to be set. It does not indicate a hardware fault and can be looked on as being an over-range function.)

590 Main RAM faulty

This would prevent the instrument from running the main instrument software. Check for dry joints on the RAM, IC6 on control board AB1, and replace the chip if necessary.

591 Main PROM faulty

This would probably never get reported since if the main PROM is faulty then, depending on the amount of corruption, the instrument probably would not run at all, i.e. the screen would stay blank. Since the PROM is socketed, try a different PROM, IC5 on control board AA1.

Chapter 6

REPLACEABLE PARTS

Contents

Introduction	6-2
Parts lists	6-2
Boards and units	6-2
Component values.....	6-2
Component spares and assemblies.....	6-2
Ordering	6-3
Electrical components.....	6-5
A0 Common parts	6-5
A1 RF tray.....	6-6
A2 AC power supply.....	6-6
A3 Front panel exit.....	6-6
A4 Attenuator.....	6-7
A5 TCXO standard	6-7
A6 Option 2, AC/DC power supply	6-7
A7 Option 1, No attenuator.....	6-8
A8 Option 3, High power attenuator	6-8
A9 Option 5, Rear panel exit.....	6-8
A10 Option 4, OCXO standard.....	6-8
A11 Option 7, Fast pulse modulation.....	6-9
A12 Option 100, Internal pulse generator	6-9
A13 Option 11, Fast pulse and high power	6-9
AA1 RF board.....	6-11
AA2 Attenuator board.....	6-49
AA2/1 High power attenuator board	6-54
AA2/2 Signal output board	6-61
AA2/5 Fast pulse modulator board	6-62
AA2/7 Fast pulse and high power board	6-68
AB1 Control board	6-77
AC1 Backlight inverter board.....	6-95
Miscellaneous mechanical parts.....	6-96

List of figures

Fig. 6-1 Boards and units fitted to the 2023 and 2024 Signal Generators.....	6-4
Fig. 6-2 Miscellaneous mechanical parts	6-96

Introduction

Each sub-assembly or printed circuit board in this equipment has been allocated a reference designator code, e.g. A0, A1, A2 etc.

The complete component reference includes its reference designator as a prefix e.g. A2C1 (capacitor C1 on sub-assembly A2) but for convenience in the text and diagrams, the prefix is omitted unless it is needed to avoid confusion. However, when ordering replacements or in correspondence, the complete component reference should be quoted.

Parts lists

The replaceable parts lists for the 2023 and 2024 Signal Generators are arranged in the following order:

- (1) A top level parts list, A0, showing parts common to all instruments.
- (2) List of parts, A1 to A5, provided in the standard version of the instruments.
- (3) Lists of parts, A6 to A13, providing the various options, e.g. A6 is the optional AC/DC power supply unit which replaces the standard AC power supply unit A2.
- (4) List of components used on units and boards AA1 onwards in alphabetical order.

Boards and units

To find out which boards and units are fitted in your instrument refer to Fig. 6-1.

Component values

One or more of the components fitted in the equipment may differ from those listed in this chapter (see *Supply statement* below).

Components indicated by an * (or SIC) have their values selected during test to achieve particular performance limits.

When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value of component as that found in the equipment.

Component spares and assemblies

Supply statement

- (a) IFR satisfies its material requirements by purchasing components from leading suppliers, who may manufacture in many countries. In most instances, components with different identities and slightly different specifications will be acceptable to us and will be identified under a single IFR part number regardless of manufacturer.

The IFR part number is the definitive reference. Service manuals and recommended service parts lists will give an example of one of the manufacturer's devices that meets our specification requirement.

We reserve the right to supply in manufactured equipment or for service spares any item that meets the requirements of our part number.

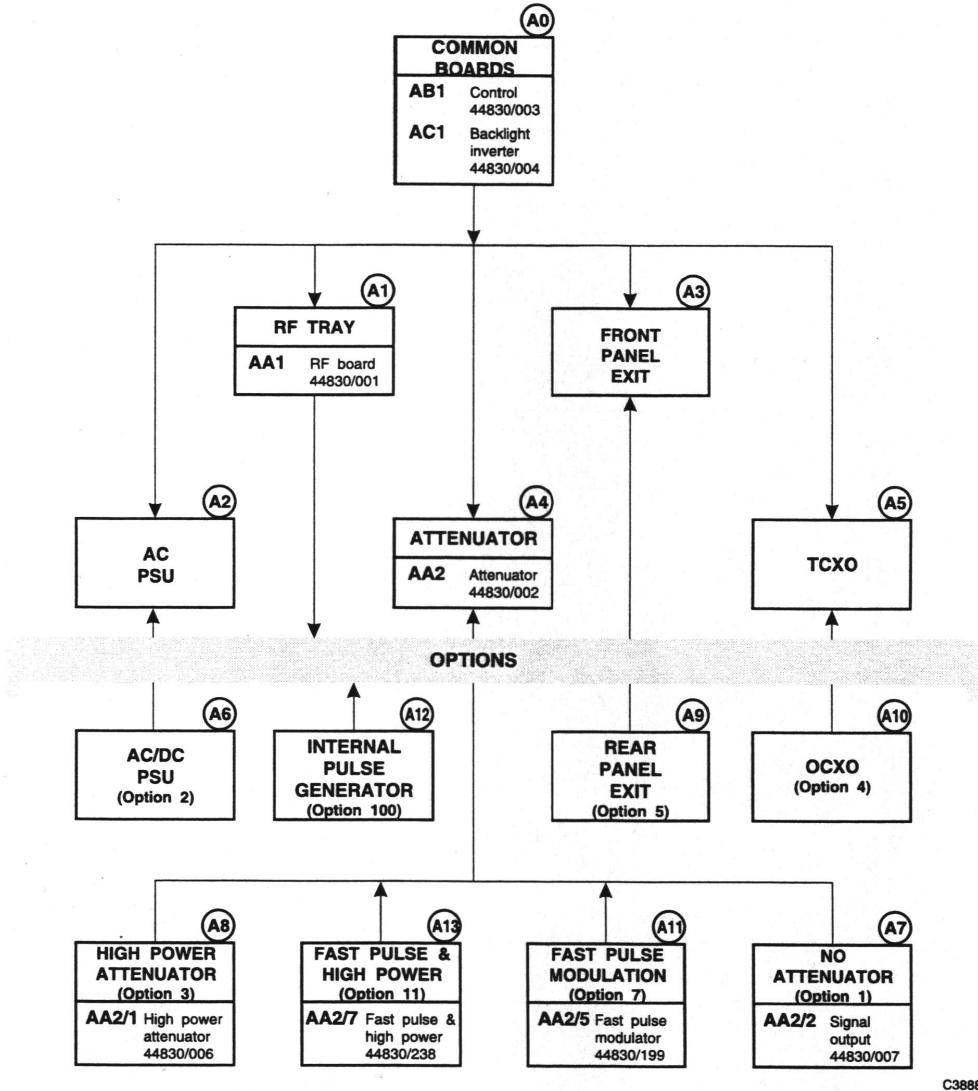
- (b) It may be necessary (due for example to obsolescence) to supply an item with a different IFR part number from that identified in our published documentation. Supply of such an alternative item is deemed to satisfy, in full, the requirements of any order or contract.

IFR Ltd warrants that the devices supplied under our part numbers will function correctly when placed in the correctly identified circuit locations for such devices in the relevant product.

Ordering

When ordering replacements, address the order to our Service Division (address at rear of manual) or nearest agent and specify the following for each component required:-

- Type and serial number of equipment, as given on the serial number label at the rear of the equipment. If this is superseded by a model number label, quote the model number instead of the type number.
- Complete circuit reference.
- Description.
- Part number.



C3888

Fig. 6-1 Boards and units fitted to the 2023 and 2024 Signal Generators

Electrical components

A0 Common parts

Issue 031

Refer to Fig. 7-1, A0 interconnections.

When ordering, prefix circuit reference with A0.

Cir. Ref.	IFR part number	Description	Manufacturer	Manufacturer's part number
	44533/446	IC-PROGRAMMED EPROM, SET OF 1, 2023, INSTRUMENT IC5 ON AB1	IFR LTD	
	43129/003	CABLE ASSEMBLY MAINS LEAD, SIDE ENTRY, BLACK, 2.5M	IFR LTD	
	43138/610	RF-CABLE-FLEXIBLE RG178B/U, 50 OHMS, MMCX MALE 10 MHZ STD, PLG AB1 to PLAB AA1	IFR LTD	
	43138/612	RIBBON LEAD 26 WAY, SOCKET 26 WAY, - D - TYPE SOCKET PLD AB1 to RF TRAY	IFR LTD	
	43138/613	RIBBON-LEAD 40 WAY, SOCKET 40 WAY, 2-OFF, - SOCKET PLH AB1 to FRONT PANEL	IFR LTD	
	43138/880	WIRE-LEAD-CRIMPED 4 WIRE, 7/0.2mm, CRIMP HOUSING ENCODER	IFR LTD	
	43138/629	WIRE-LEAD-CRIMPED 1 WIRE, 24/0.2mm, RING TERMINAL, MAINS EARTH	IFR LTD	
	44830/003	PCB-ASSEMBLY MIXED TECHNOLOGY, 2023, AB1, CONTROL	IFR LTD	
	44830/004	PCB-ASSEMBLY MIXED TECHNOLOGY, 2023, AC1, INVERTER	IFR LTD	
	46662/544	KEYBOARD PANEL, 2023, MARKED, 37 SWITCHES	IFR LTD	
	43138/616	FAN AXIAL-FLOW, BRUSHLESS, ASSEMBLY, 5V DC	IFR LTD	
	23411/060	FUSE TIME-LAG 2A RATING, 20mm LONG x 5mm DIA, 250V	LITTELFUSE TRACOR	213002.
	23423/177	CONNECTOR MAINS, PLUG, 3 WAY, RF FILTER, SINGLE	SCHAFFNER EMC LTD	FN365-4/01
	23435/121	CONNECTOR MULTIWAY, PCB HEADER, 36 WAY, STRAIGHT, FRONT PANEL	BERG ELECTRONICS	75160-102-36
	23435/564	CONNECTOR-PART SCREW-LOCK KIT, D-TYPE, AB1 to RF TRAY	3M UK PLC	3342-1
	23437/809	CONNECTOR-PART SCREW-LOCK KIT, D-TYPE, JACK SOCKET RS-232	ITT CANNON (UK)	D20418-50
	23467/264	MODULE OPTO SHAFT ENCODER, 64 CYCLES/REV, 5V 26mA	HEWLETT-PACKARD	HRPG-AS64-
	28624/227	DISPLAY LIQUID CRYSTAL, BLUE, WITH CONTROL CCT,	OPTREX (JAPAN)	DMF5010NB-FW
	13880/203	GASKET-RF CORED-KNITTED-WIRE, MONEL, 0.089mm WIRE,	CHOMERICS	01-0901-6601
	18150/225	GASKET-RF CONDUCTIVE ELASTOMER, ROUND, SOLID,	CHOMERICS	10-04-2561-1285/100M
	15310/701	GASKET-RF CORED-KNITTED-WIRE, COPPER, SILVER	KNITMESH LTD	8508
	18150/227	GASKET-RF CONDUCTIVE ELASTOMER, ROUND, TUBE	KEMTRON INTERNATIONAL	EB-1D/1-027

REPLACEABLE PARTS

Cir. Ref.	IFR part number	Description	Manufacturer	Manufacturer's part number
A1 RF tray			Issue 022	
When ordering, prefix circuit reference with A1.				
44991/173M		Complete unit		
44830/001		PCB-ASSEMBLY RF BOARD AA1	IFR LTD	
23435/562		CONNECTOR-PART SCREW-LOCK KIT, D-TYPE, JACK SOCKET RF TRAY	3M UK PLC	3341-1L
23437/037		CONNECTOR D-TYPE, PLUG, 25 WAY, PI-FILTERED, RF TRAY FROM AB1	SPECTRUM CONTROL USA	56-721-003-L1
23444/331		CONNECTOR-RF SMB-TYPE MALE, RECEPTACLE, 50 OHMS, PLAB	ITT CANNON (UK)	051-045-0000-910
23444/512		CONNECTOR-RF SMA-TYPE FEMALE, JACK, 50 OHMS, RF OUT FROM RF TRAY	ITT CANNON (UK)	050-645-9039-890
23437/829		CONNECTOR-PART GASKET, D-TYPE, 25 WAY, RF/EMC,	KEMTRON INTERNATIONL	PA-3J-023/
13860/104		GASKET-RF LINEAR-FINGER-STRIP, SINGLE-EDGED,	TECKNIT EUROPE LTD	55-45507
18150/227		GASKET-RF CONDUCTVE ELASTOMER, ROUND, TUBE,	KEMTRON INTERNATIONL	EB-1D/1-027

A2 AC power supply

Issue 005

When ordering, prefix circuit reference with A2.

43138/627		WIRE-LEAD-CRIMPED 6 WIRE, 16,24/0.2mm & SCRND, MAINS INPUT	IFR LTD	
43138/628		WIRE-LEAD-CRIMPED 16 WIRE, 7 & 16/0.2mm, 1.14mm POWER SUPPLY	IFR LTD	
23488/559		THERMOSTAT OPEN-ON-RISE 80 +/- 4 DEG.C, 15 DEG.C	ELMWOOD SENSORS LTD	2455R-82-872-L80C
23725/609		POWER-SUPPLY SWITCH MODE UNIT, OPEN FRAME, 60W, 85-264 V AC INPUT	COUTANT LAMBDA	HVI-60-47A

A3 Front panel exit

Issue 001

When ordering, prefix circuit reference with A3.

43138/611		RF-CABLE-SEMI-RIGID UT141, 50 OHMS, SMA MALE RF OUTPUT	IFR LTD	
43138/617		RF-CABLE-FLEXIBLE RG178B/U, 50 OHMS, BNC FEMALE MOD INPUT	IFR LTD	
43138/618		RF-CABLE-FLEXIBLE RG178B/U, 50 OHMS, BNC FEMALE LF OUTPUT	IFR LTD	

Cir. Ref.	IFR part number	Description	Manufacturer	Manufacturer's part number
A4 Attenuator			Issue 007	
When ordering, prefix circuit reference with A4.				
43138/614		RIBBON-LEAD 16 WAY, SOCKET 16 WAY, - UNTERMINATED, RF TRAY PLAE	IFR LTD	
44830/002		PCB-ASSEMBLY MIXED TECHNOLOGY, 2023/3001, AA2,	IFR LTD	
23642/922		FILTER RFI-SUPPRESSION, 12nF MIN, 50V DC,	FERROPERM UK LTD	128,88XXX-94506
A5 TCXO standard			Issue 002	
When ordering, prefix circuit reference with A5.				
28313/892		OSCILLATOR CRYSTAL, 10 MHz +/- 0.5 ppm, TCXO, 5V,	MCKNIGHT CRYSTALS	DFA36HV 10MHz A36036
A6 Option 2, AC/DC power supply			Issue 003	
When ordering, prefix circuit reference with A6.				
43130/119		WIRE-LEAD-CRIMPED 2 WIRE, 63/0.2mm, 2.13mm TERM DC INPUT (EXT)	IFR LTD	
43138/631		WIRE-LEAD-CRIMPED 8 WIRE, 7/0.2mm & SCREENED, MAINS INPUT	IFR LTD	
43138/632		WIRE-LEAD-CRIMPED 14 WIRE, 7 & 16/0.2mm, 1.14mm POWER SUPPLY	IFR LTD	
43138/678		WIRE-LEAD-CRIMPED 2 WIRE, 32/0.2mm, 2.1mm TERM DC INPUT	IFR LTD	
43138/679		WIRE-LEAD-CRIMPED 1 WIRE, 32/0.2mm, RECEPTACLE FUSE	IFR LTD	
43138/680		WIRE-LEAD-CRIMPED 1 WIRE, 32/0.2mm, RECEPTACLE EARTH	IFR LTD	
43138/681		WIRE-LEAD-CRIMPED 1 WIRE, 24/0.2mm, RECEPTACLE EARTH	IFR LTD	
23411/074		FUSE TIME-LAG 10A RATING, 20mm LONG x 5mm DIA,	SCHURTER SWITZERLAND	SPT-0001-2514
23635/845		CORE BEAD, 8mm DIA, 10mm LONG, 3mm I/DIA, FERRITE,	PHILIPS	4330-030-33200
26346/120		CAPACITOR-FIXED CERAMIC 10nF +/-20% 50V X7R	PHILIPS	A41C 103K-DRM
26582/421		CAPACITOR-FIXED POLYESTER 4.7uF +/-10% 63V RADIAL,	VISHAY COMPONENTS	MKT-1822-547/065
44991/179		POWER SUPPLY SWITCH MODE UNIT, 180-264 V AC OR 90-132 VAC AND 11-32 VDC	IFR LTD	

REPLACEABLE PARTS

Cir. Ref.	IFR part number	Description	Manufacturer	Manufacturer's part number
A7 Option 1, No attenuator			Issue 006	
When ordering, prefix circuit reference with A7.				
44830/007		PCB-ASSEMBLY CONVENTIONAL, 2023/3001, AA2/2,	IFR LTD	
A8 Option 3, High power attenuator			Issue 008	
When ordering, prefix circuit reference with A8.				
43138/614		RIBBON-LEAD 16 WAY, SOCKET 16 WAY, - UNTERMINATED, RF TRAY PLAE	IFR LTD	
44830/006		PCB-ASSEMBLY MIXED TECHNOLOGY, 2023/3001, AA2/1,	IFR LTD	
23642/922		FILTER RFI-SUPPRESSION, 12nF MIN, 50V DC,	FERROPERM UK LTD	128,88XXX-94506
A9 Option 5, Rear panel exit			Issue 003	
When ordering, prefix circuit reference with A9.				
43138/630		RF-CABLE-SEMI-RIGID UT141, 50 OHMS, SMA MALE RF OUTPUT	IFR LTD	
22315/812		GROMMET BLIND, 12.7 mm PANEL HOLE, 14.7 mm O/DIA, FRONT PANEL HOLES	HEYCO MANUFACTURING	440-2491-BLACK
23188/373		GROMMET BLIND, 15.9 mm PANEL HOLE, 18.2 mm O/DIA, FRONT PANEL HOLES	HEYCO MANUFACTURING	440-2497-BLACK
23443/855		CONNECTOR-RF BNC-TYPE FEMALE, RECEPTACLE, 50 OHMS, CONTROL BOARD I/O's	AMPHENOL LTD	31-5640-2010
A10 Option 4, OCXO standard			Issue 001	
When ordering, prefix circuit reference with A10.				
28313/883		OSCILLATOR CRYSTAL, 10 MHz +/- 0.1 ppm, OCXO, 12V,	NDK CO LTD	END3032A

Cir. Ref.	IFR part number	Description	Manufacturer	Manufacturer's part number
A11 Option 7, Fast pulse modulation			Issue 009	
When ordering, prefix circuit reference with A11.				
43138/614		RIBBON-LEAD 16 WAY, SOCKET 16 WAY, UNTERMINATED FILTERS TO ATTEN	IFR LTD	
43138/864		RF-CABLE-FLEXIBLE RG178B/U 50 OHMS, SMB MALE PULSE INPUT TO PCB	IFR LTD	
44830/199		PCB-ASSEMBLY MIXED TECHNOLOGY, 2023 AA2/5, FAST	IFR LTD	
46662/618		KEYBOARD PANEL, 2023 OP7 MARKD, 37 SWITCHES REPLACES 46662/544 ON A0	IFR LTD	
43138/618		RF-CABLE-FLEXIBLE RG178B/U, 50 OHMS, BNC FEMALE MOD I/O	IFR LTD	
43138/865		RF-CABLE-FLEXIBLE RG178B/U, 50 OHMS, SMB FEMALE PULSE INPUT	IFR LTD	
23642/922		FILTER RFI-SUPPRESSION, 12nF MIN, 50V DC	AMP (GB) LTD	128.88xxx-94506
18150/227		GASKET-RF CONDUCTIVE ELASTOMER, ROUND, TUBE,	KEMTRON INTERNATIONAL	EB-1D/1-027
23642/959		FILTER RFI-SUPPRESSION, 1nF MIN, 100V DC, 5A	FERROPERM UK LTD	138.62001
18720/651		GASKET-RF CONDUCTIVE ELASTOMER, STRIP, EXPANDED	W.L.GORE & ASSOCIATE	EDR-21-020-0250-SC

A12 Option 100, Internal pulse generator

Issue 002

When ordering, prefix circuit reference with A12.

44533/446	IC_PROGRAMMED EPROM, SET OF 1, 2023 INSTRUMENT	IFR LTD
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A13 Option 11, Fast pulse and high power

Issue 002

When ordering, prefix circuit reference with A13.

43138/614	RIBBON-LEAD 16 WAY, SOCKET 16 WAY, UNTERMINATED FILTERS TO ATTEN	IFR LTD
43138/864	RF-CABLE-FLEXIBLE RG178B/U 50 OHMS, SMB MALE PULSE INPUT TO PCB	IFR LTD
44830/238	PCB-ASSEMBLY MIXED TECHNOLOGY, 2023 AA2/7, FAST	IFR LTD
46662/618	KEYBOARD PANEL, 2023 OP7 MARKD, 37 SWITCHES REPLACES 46662/544 ON A0	IFR LTD
43138/618	RF-CABLE-FLEXIBLE RG178B/U, 50 OHMS, BNC FEMALE MOD I/O	IFR LTD
43138/865	RF-CABLE-FLEXIBLE RG178B/U, 50 OHMS, SMB FEMALE PULSE INPUT	IFR LTD
23642/922	FILTER RFI-SUPPRESSION, 12nF MIN, 50V DC	AMP (GB) LTD

128.88xxx-94506

REPLACEABLE PARTS

Cir. Ref.	IFR part number	Description	Manufacturer	Manufacturer's part number
A13 Option 11, Fast pulse and high power (continued)				
	18150/227	GASKET-RF CONDUCTIVE ELASTOMER, ROUND, TUBE,	KEMTRON INTERNATIONAL	EB-1D/1-027
	23642/959	FILTER RFI-SUPPRESSION, 1nF MIN, 100V DC, 5A	FERROPERM UK LTD	138.62001
	18720/651	GASKET-RF CONDUCTIVE ELASTOMER, STRIP, EXPANDED	W.L.GORE & ASSOCIATE	EDR-21-020-0250-SC

REPLACEABLE PARTS

Cir. Ref.	IFR part number	Description	Manufacturer	Manufacturer's part number
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Miscellaneous mechanical parts

Order without prefix. Item numbers as show in Fig. 6-2.

Item no.	Description	Part No.
1	Front panel marked (standard instrument)	46662/544
	Front panel marked (Option 7 and Option 11 instrument)	46662/618
2	Instrument cover	41590/289
3	Knob, control	37591/605
4	Collet	37591/452
5	Front panel handle, 1 of 2	37591/674
6	Front foot, 1 of 2	37591/643
7	Tilt foot, 1 of 2	37591/439
8	Rear foot, 1 of 2	37591/460
9	Stud, 1 of 2	37591/461
10	Rear panel stand-off 1 of 2	37591/580
11	Side handle	41700/756
12	End cap, 1 of 2	22315/584
13	Cover 1 of 2	37591/668
	[The marked rear panel is part of the main chassis.]	
	Grommet, open	23184/131

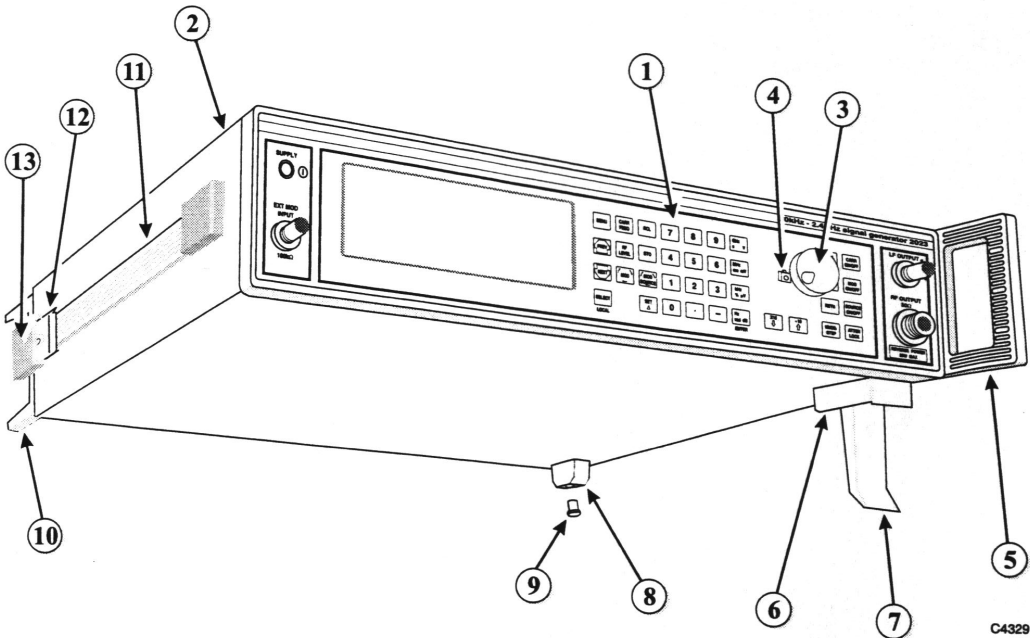


Fig. 6-2 Miscellaneous mechanical parts

Chapter 7

SERVICING DIAGRAMS

Contents

Circuit notes	7-2
Component values	7-2
Symbols	7-2
PCB layouts	7-2

List of figures

Fig. 7-1 A0 Interconnections	7-3
Fig. 7-2 AA1 RF board: Component layout (component side)	7-4
Fig. 7-3 AA1 RF board: Component layout (solder side)	7-5
Fig. 7-4 AA1 RF board: Sheet 1 component locations	7-6
Fig. 7-5 AA1 RF board: Carrier generation circuit	7-7
Fig. 7-6 AA1 RF board: Sheet 2 component locations	7-8
Fig. 7-7 AA1 RF board: VCXO loop circuit	7-9
Fig. 7-8 AA1 RF board: Sheet 3 component locations	7-10
Fig. 7-9 AA1 RF board: Synthesizer circuit	7-11
Fig. 7-10 AA1 RF board: Sheet 4 component locations	7-12
Fig. 7-11 AA1 RF board: Loop filter and autocal circuit	7-13
Fig. 7-12 AA1 RF board: Sheet 5 component locations	7-14
Fig. 7-13 AA1 RF board: FM drive circuit	7-15
Fig. 7-14 AA1 RF board: Sheet 6 component locations	7-16
Fig. 7-15 AA1 RF board: Level modulator circuit	7-17
Fig. 7-16 AA1 RF board: Sheet 7 component locations	7-18
Fig. 7-17 AA1 RF board: Frequency generator circuit	7-19
Fig. 7-18 AA1 RF board: Sheet 8 component locations	7-20
Fig. 7-19 AA1 RF board: Interface and attenuator drive circuit	7-21
Fig. 7-20 AA1 RF board: Sheet 9 component locations	7-22
Fig. 7-21 AA1 RF board: Output amplifier circuit	7-23
Fig. 7-22 AA1 RF board: Power supplies circuit	7-25
Fig. 7-23 AA2 Attenuator board: Component layout	7-26
Fig. 7-24 AA2 Attenuator board circuit	7-27
Fig. 7-25 AA2/1 High power attenuator board: Component layouts	7-28
Fig. 7-26 AA2/1 High power attenuator board: Pulse mod and attenuator circuit	7-29
Fig. 7-27 AA2/1 High power attenuator board: Power amp and RPP circuit	7-31
Fig. 7-28 AA2/2 Signal output board circuit	7-33
Fig. 7-29 AA2/5 Fast pulse modulator board: Component layouts	7-34
Fig. 7-30 AA2/5 Fast pulse modulator board: Pulse mod circuit	7-35
Fig. 7-31 AA2/5 Fast pulse modulator board: RPP and atten circuit	7-37
Fig. 7-32 AA2/7 Fast pulse and high power board: Component layouts	7-38
Fig. 7-33 AA2/7 Fast pulse and high power board: Pulse mod circuit	7-39
Fig. 7-34 AA2/7 Fast pulse and high power board: Attenuator circuit	7-41
Fig. 7-35 AA2/7 Fast pulse and high power board: Power amp and RPP circuit	7-43
Fig. 7-36 AB1 Control board: Component layout	7-45
Fig. 7-37 AB1 Control board: Sheet 1 component locations	7-46
Fig. 7-38 AB1 Control board: Microprocessor and memory circuit	7-47
Fig. 7-39 AB1 Control board: Sheet 2 component locations	7-48
Fig. 7-40 AB1 Control board: DSP audio generator circuit	7-49
Fig. 7-41 AB1 Control board: Sheet 3 component locations	7-50

contd./...

List of figures (continued)

Fig. 7-42 AB1 Control board: Interrupts and serial interface circuit7-51
 Fig. 7-43 AB1 Control board: Sheet 4 component locations7-52
 Fig. 7-44 AB1 Control board: Modulation and level circuit7-53
 Fig. 7-45 AB1 Control board: Sheet 5 component locations7-54
 Fig. 7-46 AB1 Control board: Standard selection circuit7-55
 Fig. 7-47 AB1 Control board: Sheet 6 component locations7-56
 Fig. 7-48 AB1 Control board: Interface circuit7-57
 Fig. 7-49 AB1 Control board: Sheet 7 component locations7-58
 Fig. 7-50 AB1 Control board: PSU filtering and regulation circuit7-59
 Fig. 7-51 AB1 Control board: Power supplies circuit.....7-61
 Fig. 7-52 AC1 Backlight inverter board component layout.....7-62
 Fig. 7-53 AC1 Backlight inverter board circuit7-63
 Fig. 7-54 AF1 Keyboard circuit.....7-65
 Fig. 7-55 AC/DC power supply interconnections.....7-66
 Fig. 7-56 AC/DC supply: AD-DC input circuit7-67
 Fig. 7-57 AC/DC supply: DC-DC input circuit.....7-69
 Fig. 7-58 AC/DC supply: Control circuit.....7-71
 Fig. 7-59 AC/DC supply: DC output circuit7-73

Circuit notes

Component values

Resistors :	R = ohms,	k = kilohms,	M = megohms.
Capacitor:	μ = microfarads,	n = nanofarads,	p = picofarads.
Inductors :	μ = microhenries,	m = millihenries.	
SIC :	= value selected during test, nominal value shown.		

Symbols

Symbols are to IEC617 (BS 3939) with the following additions :



Static sensitive component



Test point



Unit identification

PCB layouts

Unless otherwise stated, PCB layouts are shown as viewed from the component side.

Interconnections A0

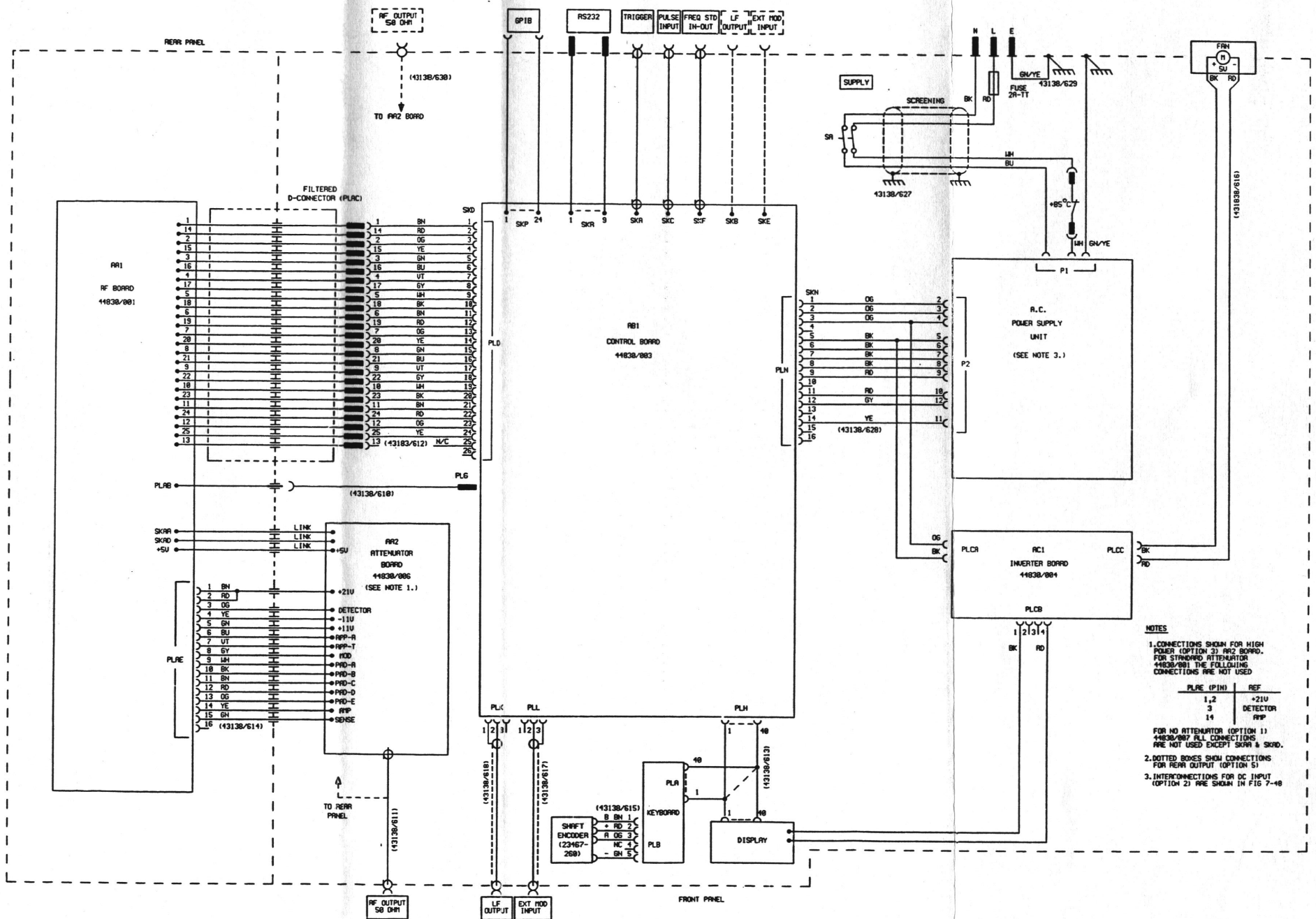


Fig. 7-1 A0 Interconnections

RF board component layout AA1

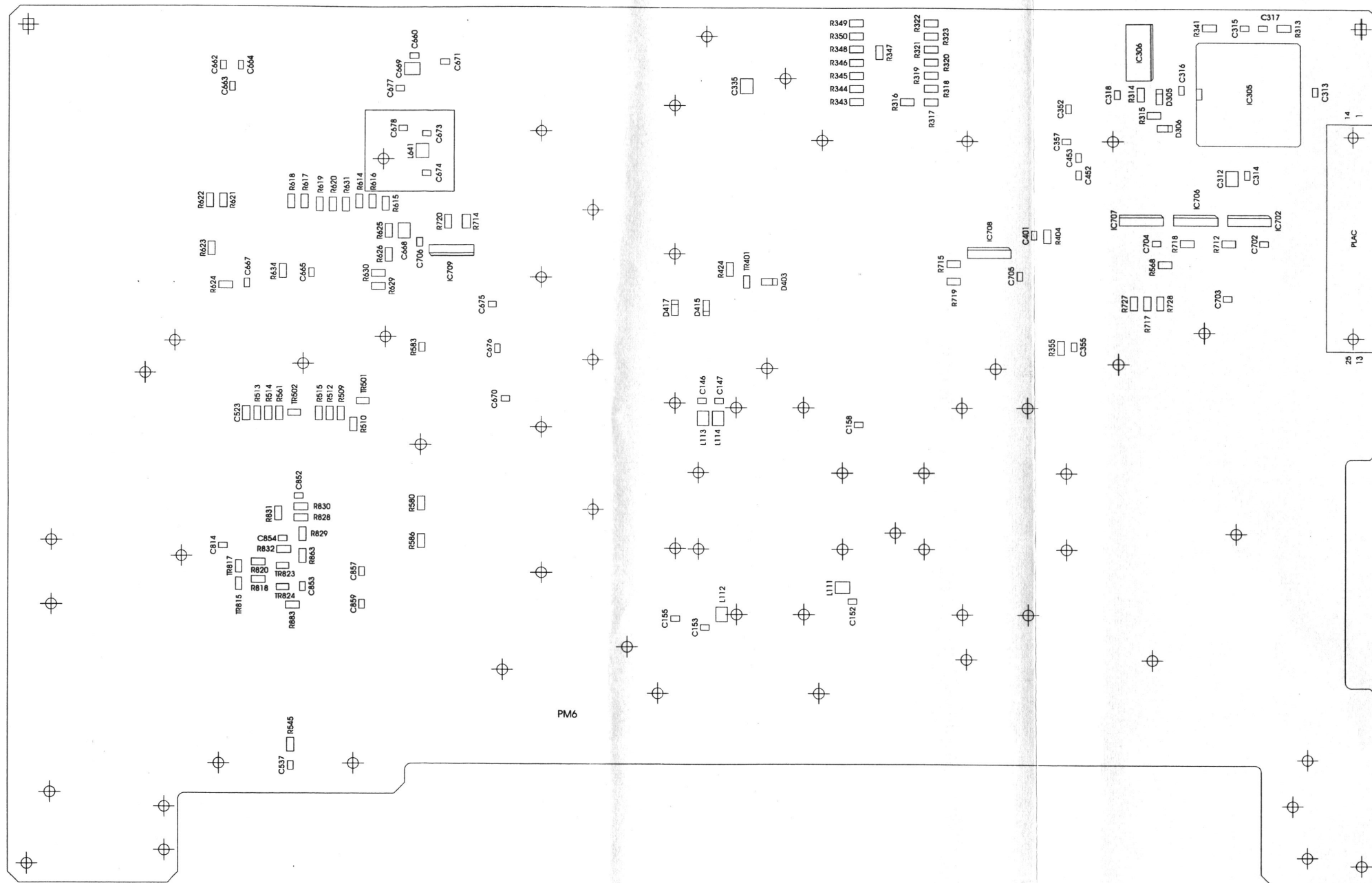
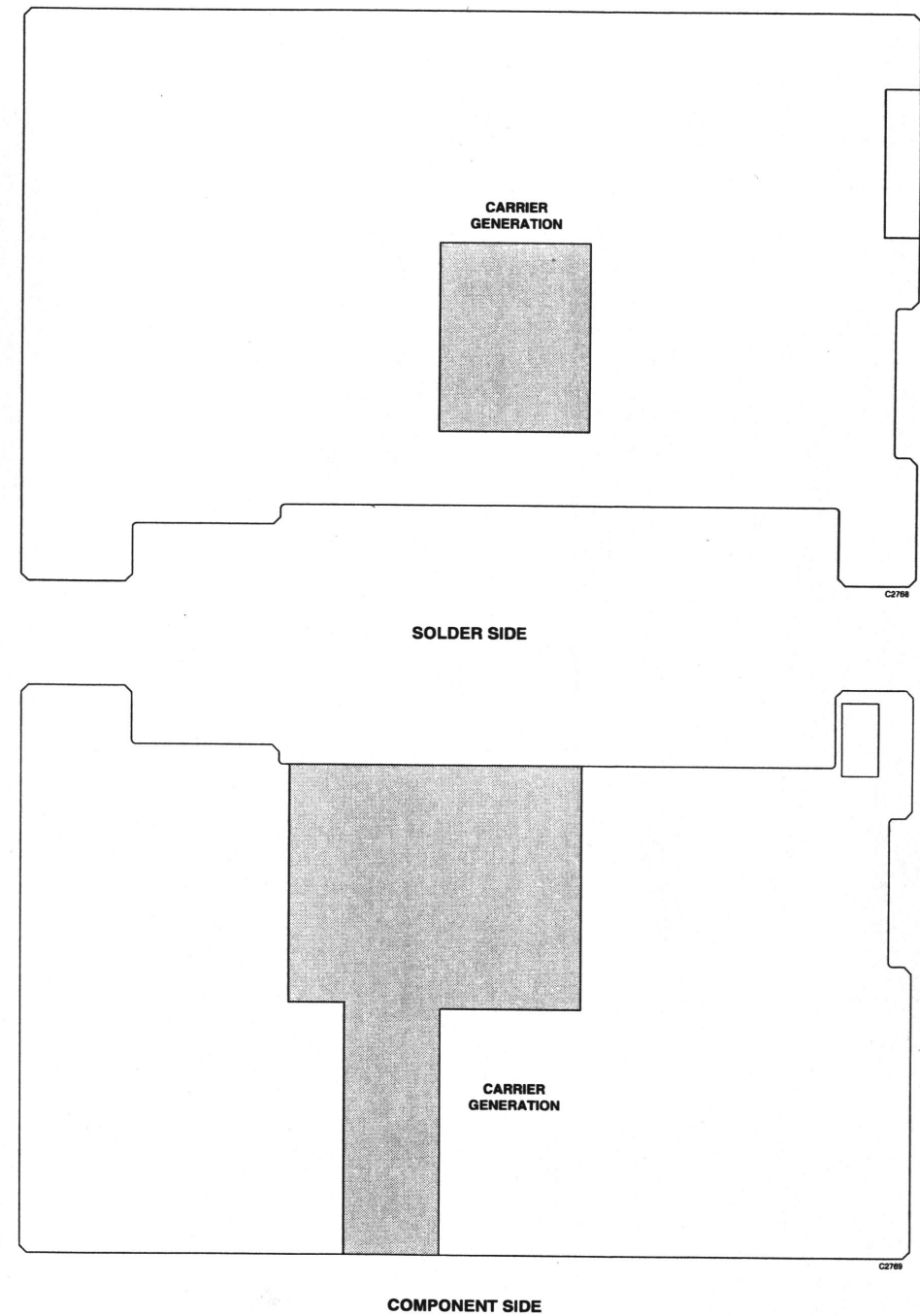


Fig. 7-3 AA1 RF board: Component layout (solder side)

Sheet 1 component locations **AA1**



RF board component layout **AA1**

Fig. 7-4 AA1 RF board: Sheet 1 component locations

Carrier generation AA1

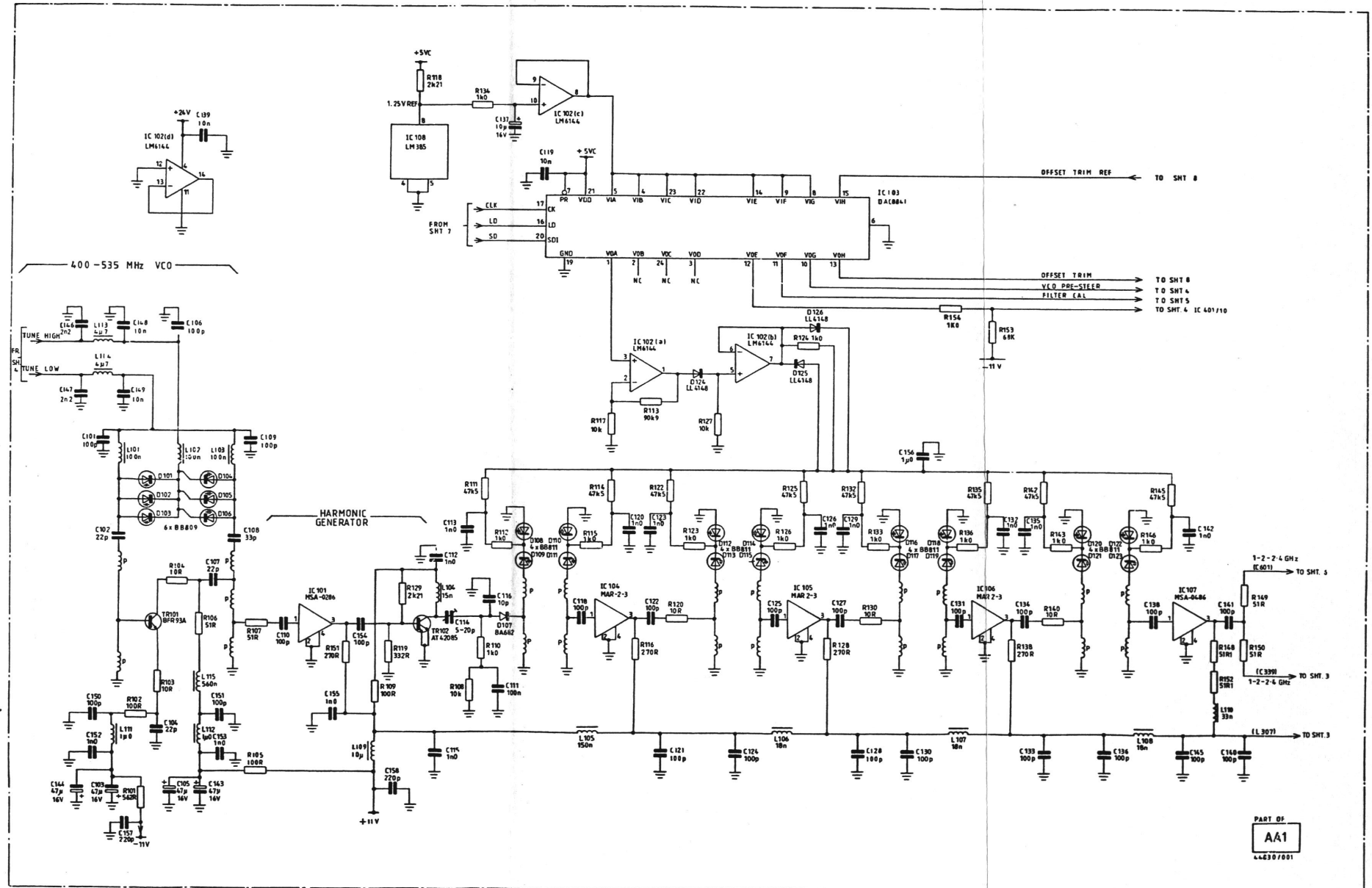
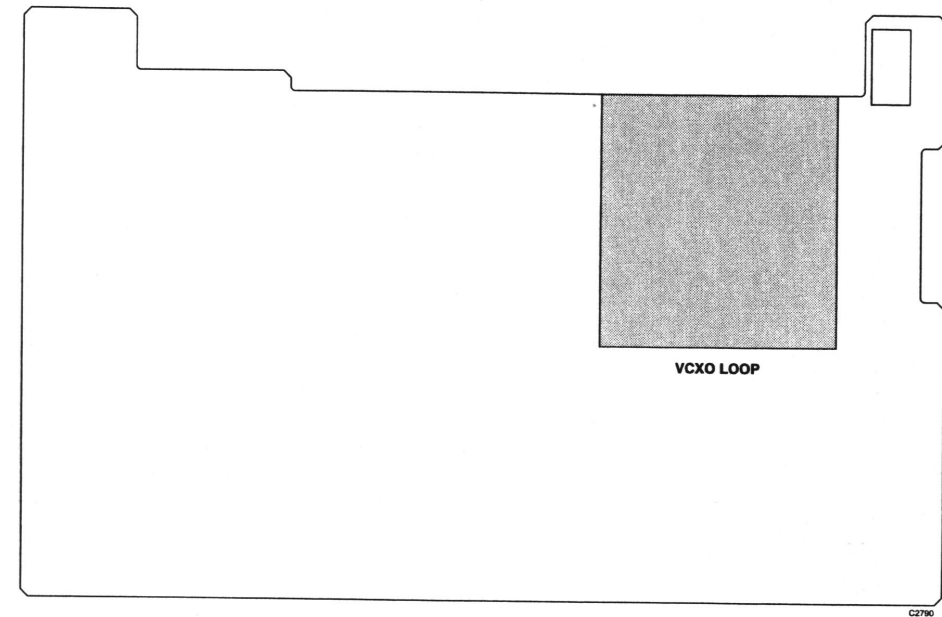


Fig. 7-5 AA1 RF board: Carrier generation circuit

Sheet 2 component locations **AA1**



COMPONENT SIDE

Carrier generation **AA1**

Fig. 7-6 AA1 RF board: Sheet 2 component locations

VCXO loop AA1

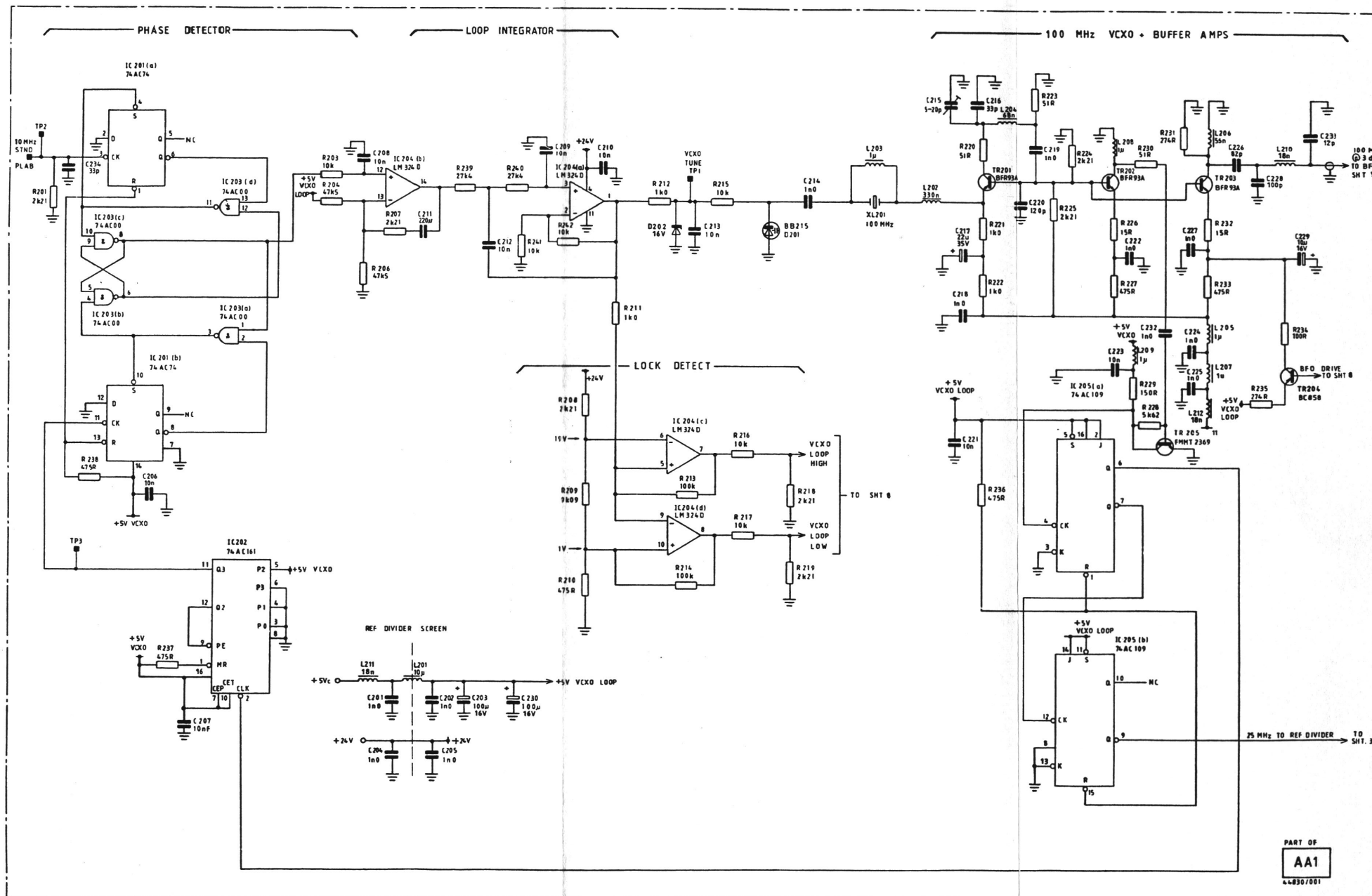
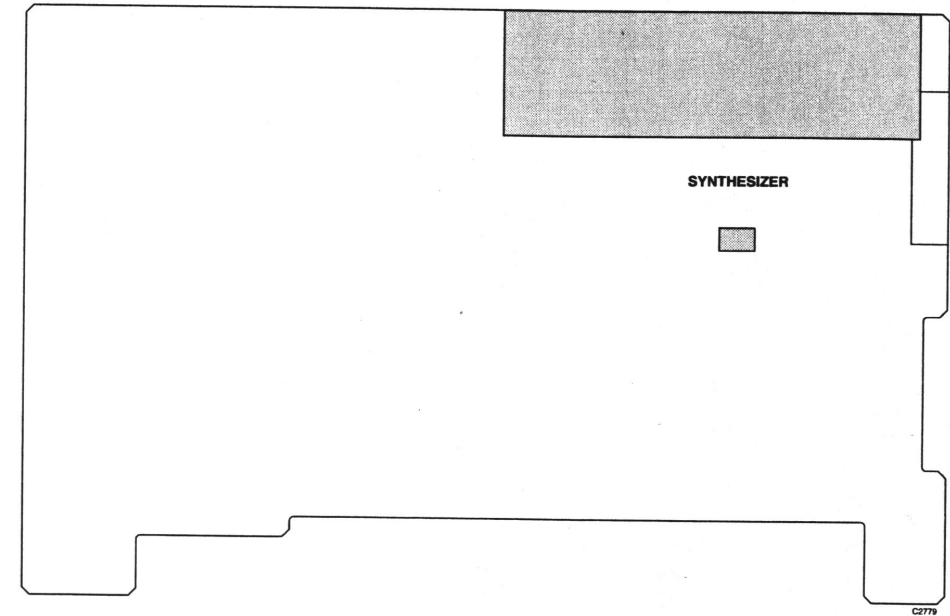
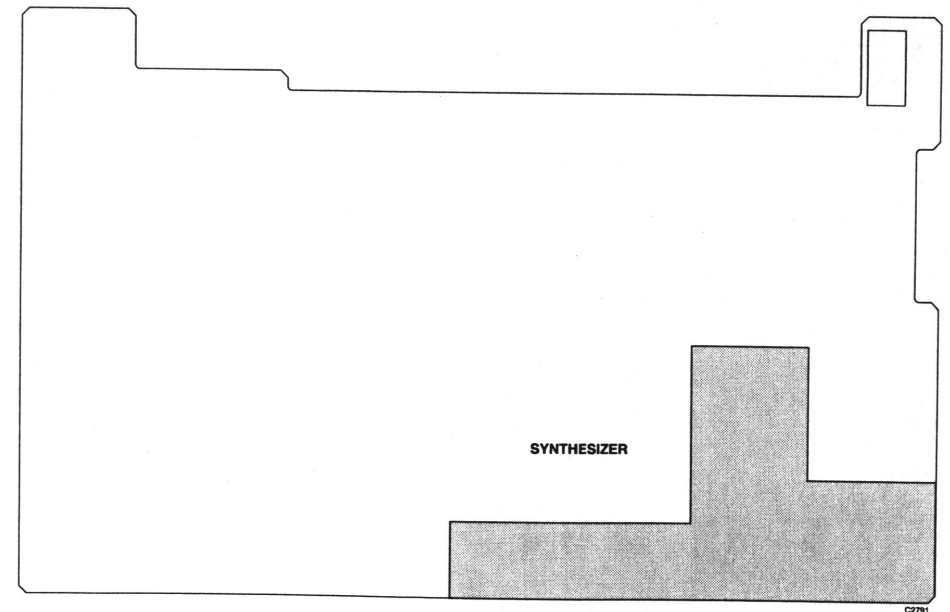


Fig. 7-7 AA1 RF board: VCXO loop circuit

Sheet 3 component locations **AA1**



SOLDER SIDE



COMPONENT SIDE

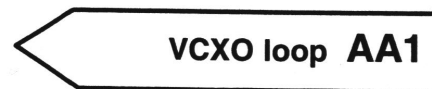


Fig. 7-8 AA1 RF board: Sheet 3 component locations

Synthesizer AA1

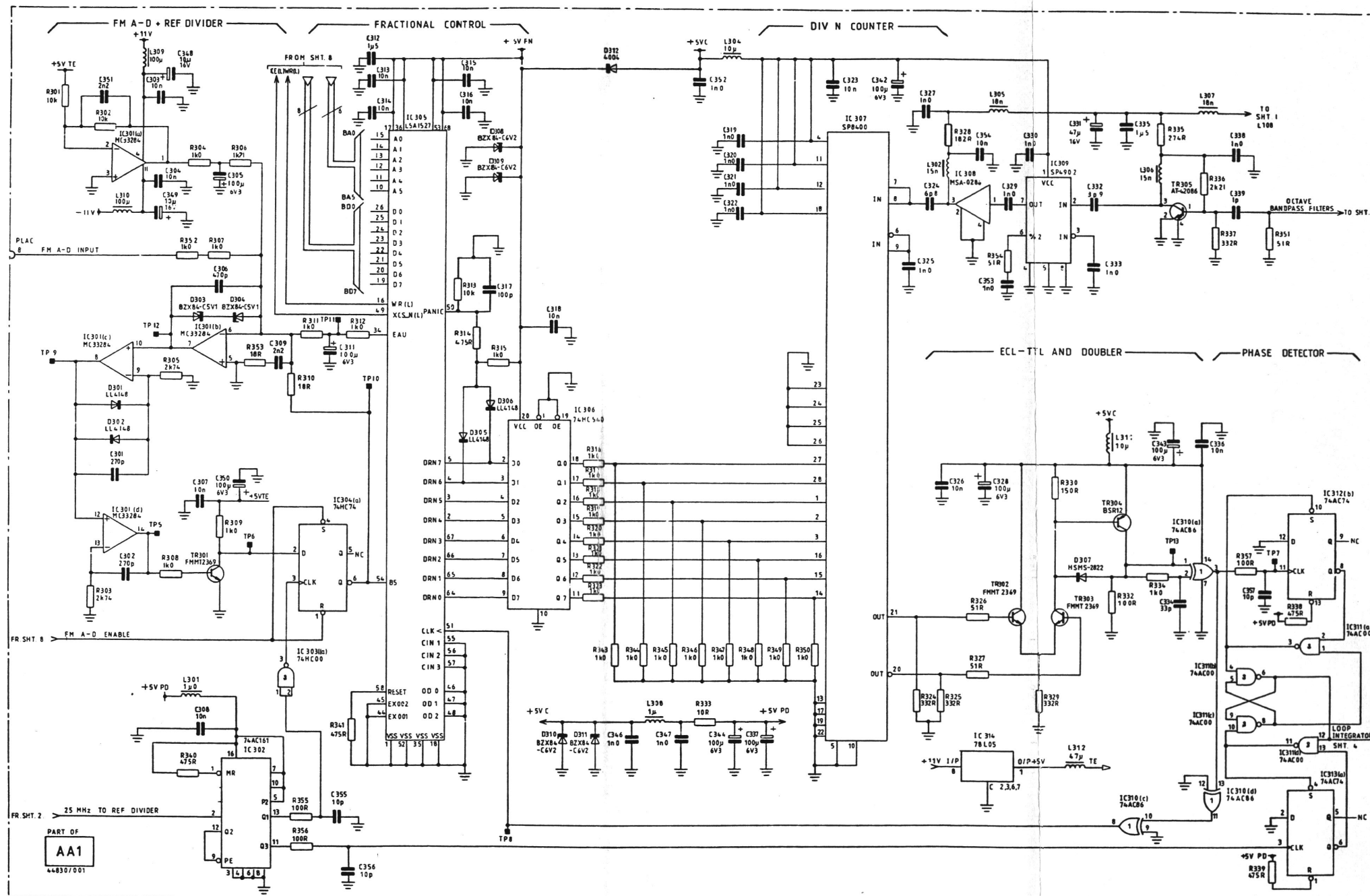
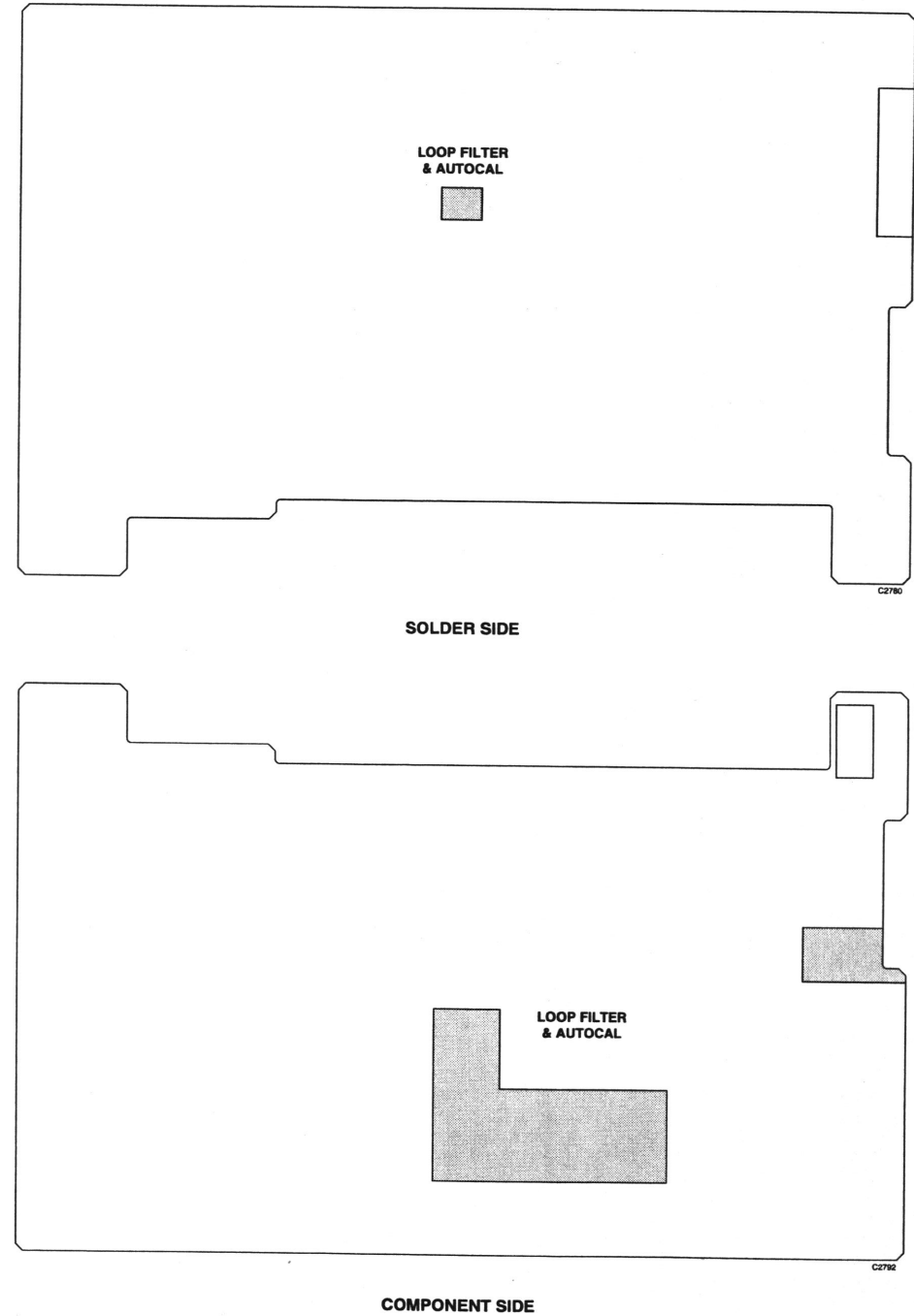


Fig. 7-9 AA1 RF board: Synthesizer circuit

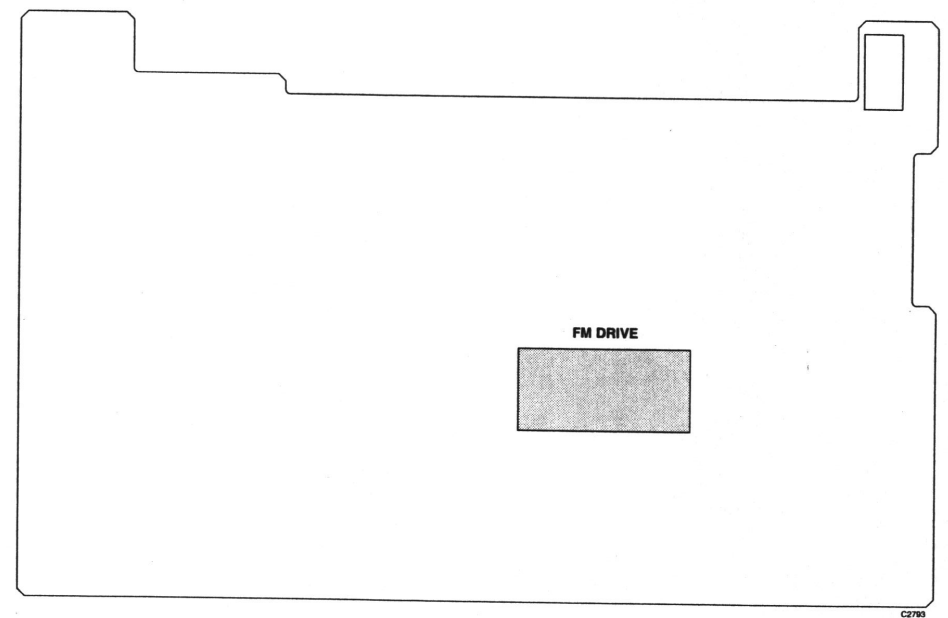
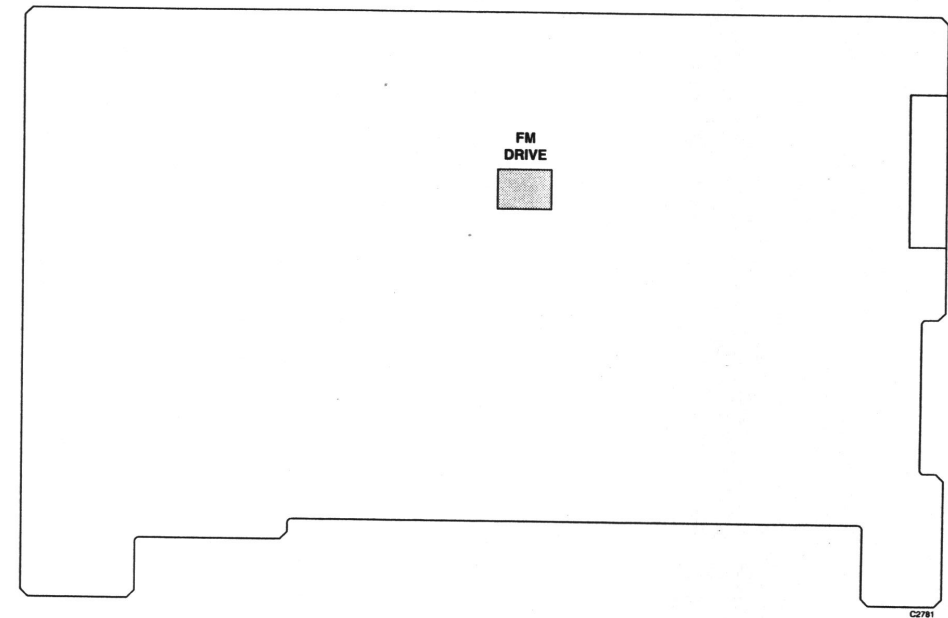
Sheet 4 component locations **AA1**



Synthesizer AA1

Fig. 7-10 AA1 RF board: Sheet 4 component locations

Sheet 5 component locations **AA1**



Loop filter and autocal **AA1**

Fig. 7-12 AA1 RF board: Sheet 5 component locations

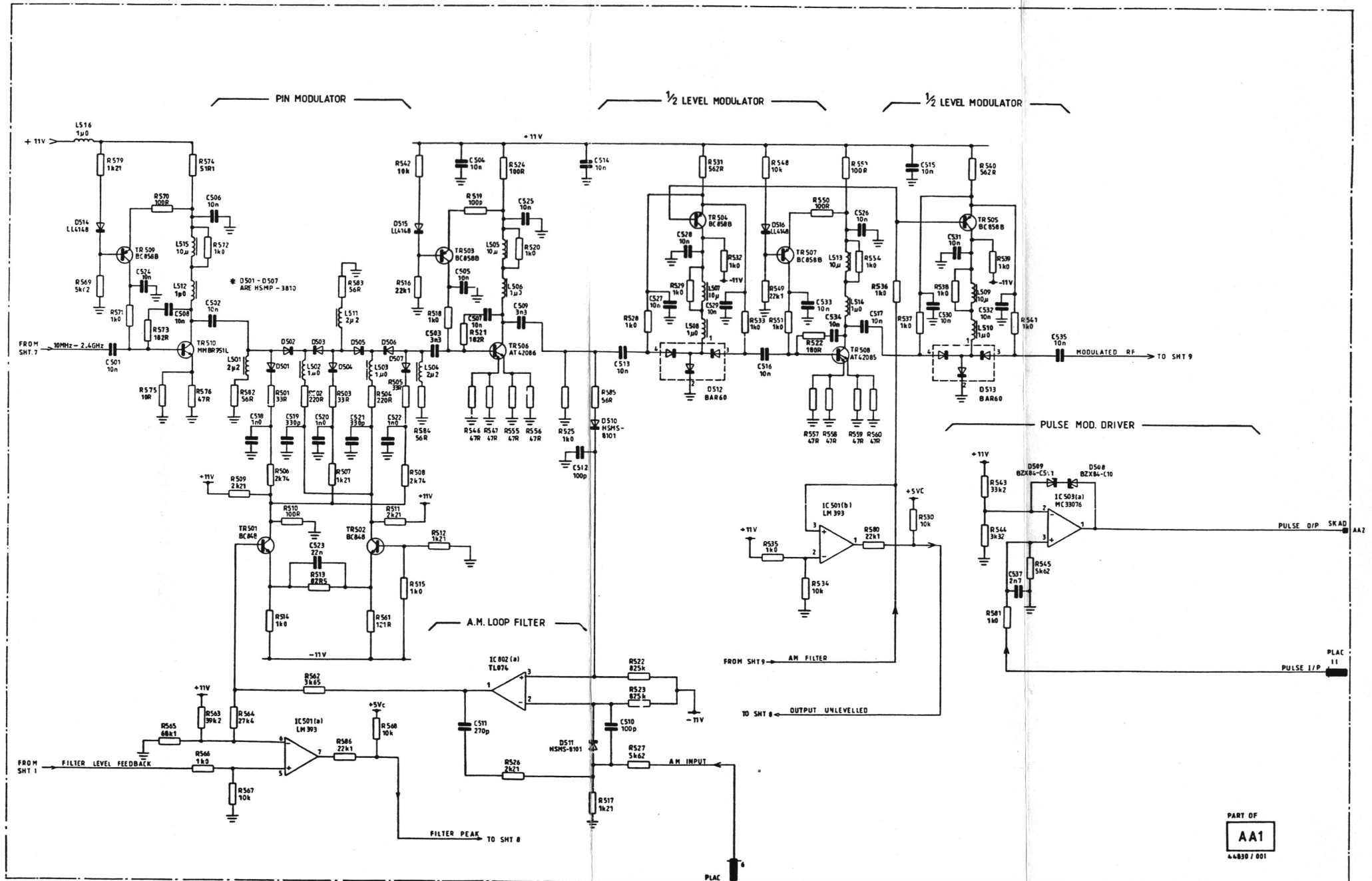
Sheet 6 component locations **AA1**



FM drive AA1

Fig. 7-14 AA1 RF board: Sheet 6 component locations

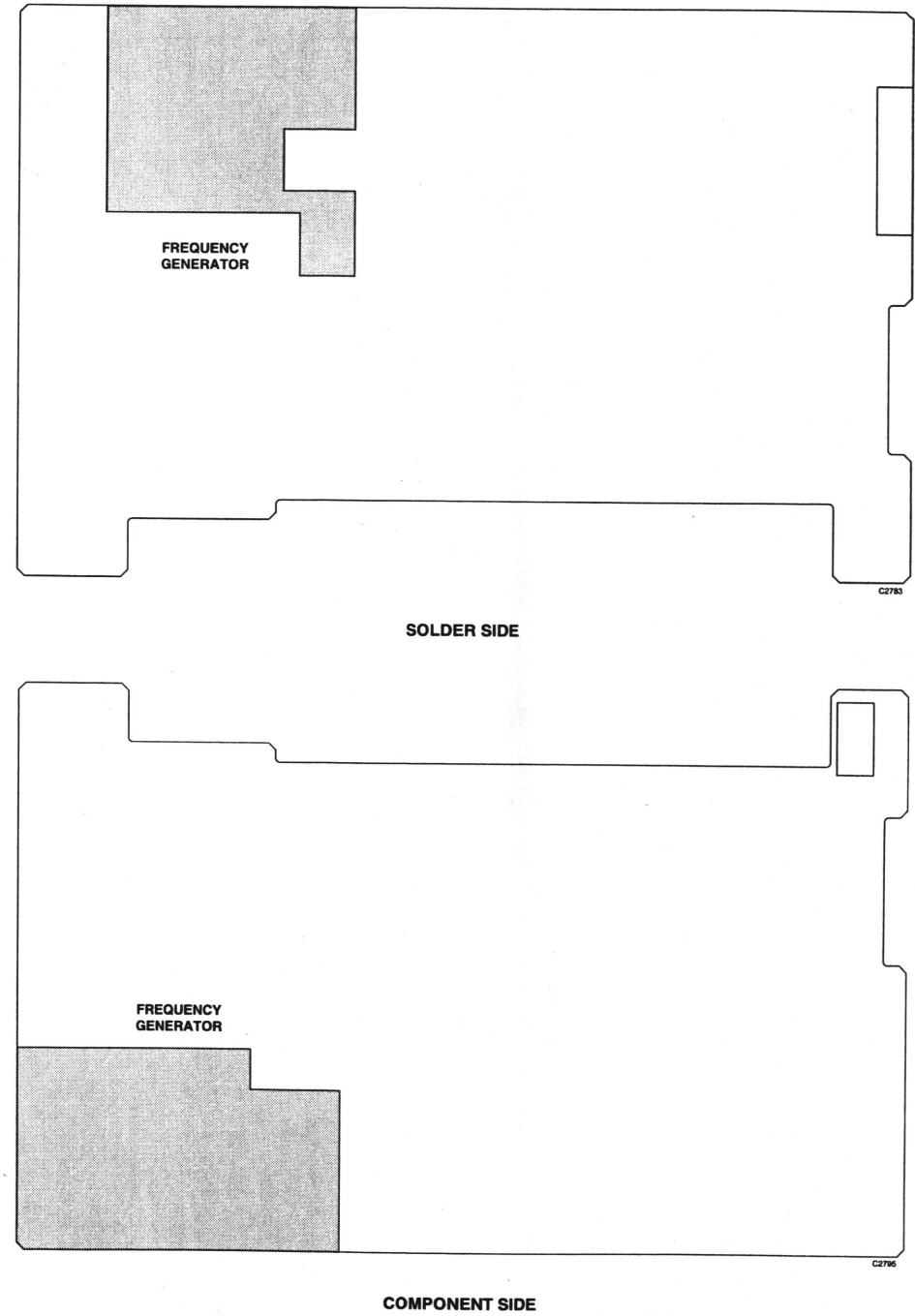
Level modulator AA1



PART OF
AA1
44830 / 001

Fig. 7-15 AA1 RF board: Level modulator circuit

Sheet 7 component locations **AA1**



Level modulator **AA1**

Fig. 7-16 AA1 RF board: Sheet 7 component locations

Frequency generator AA1

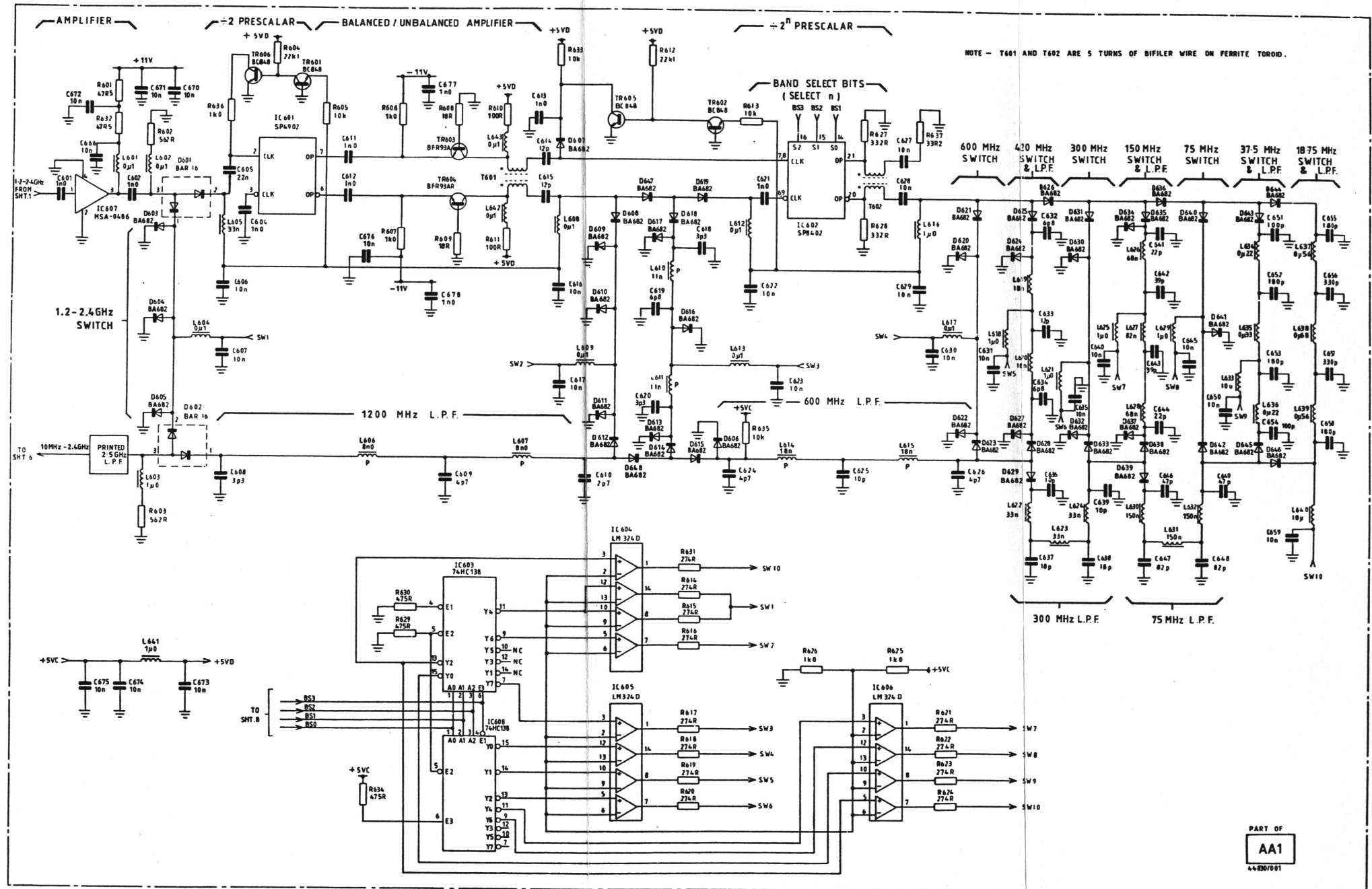
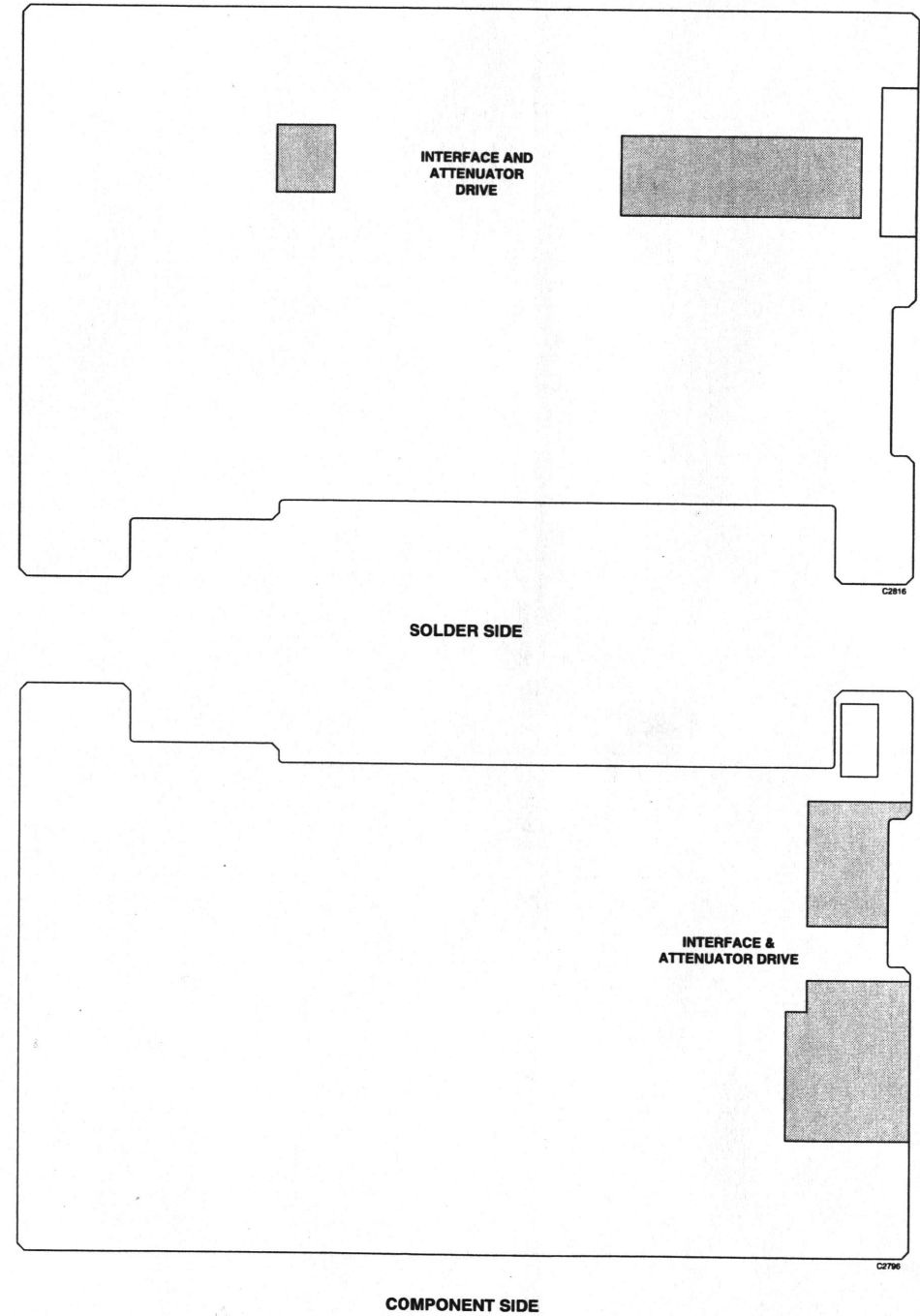


Fig. 7-17 AA1 RF board: Frequency generator circuit

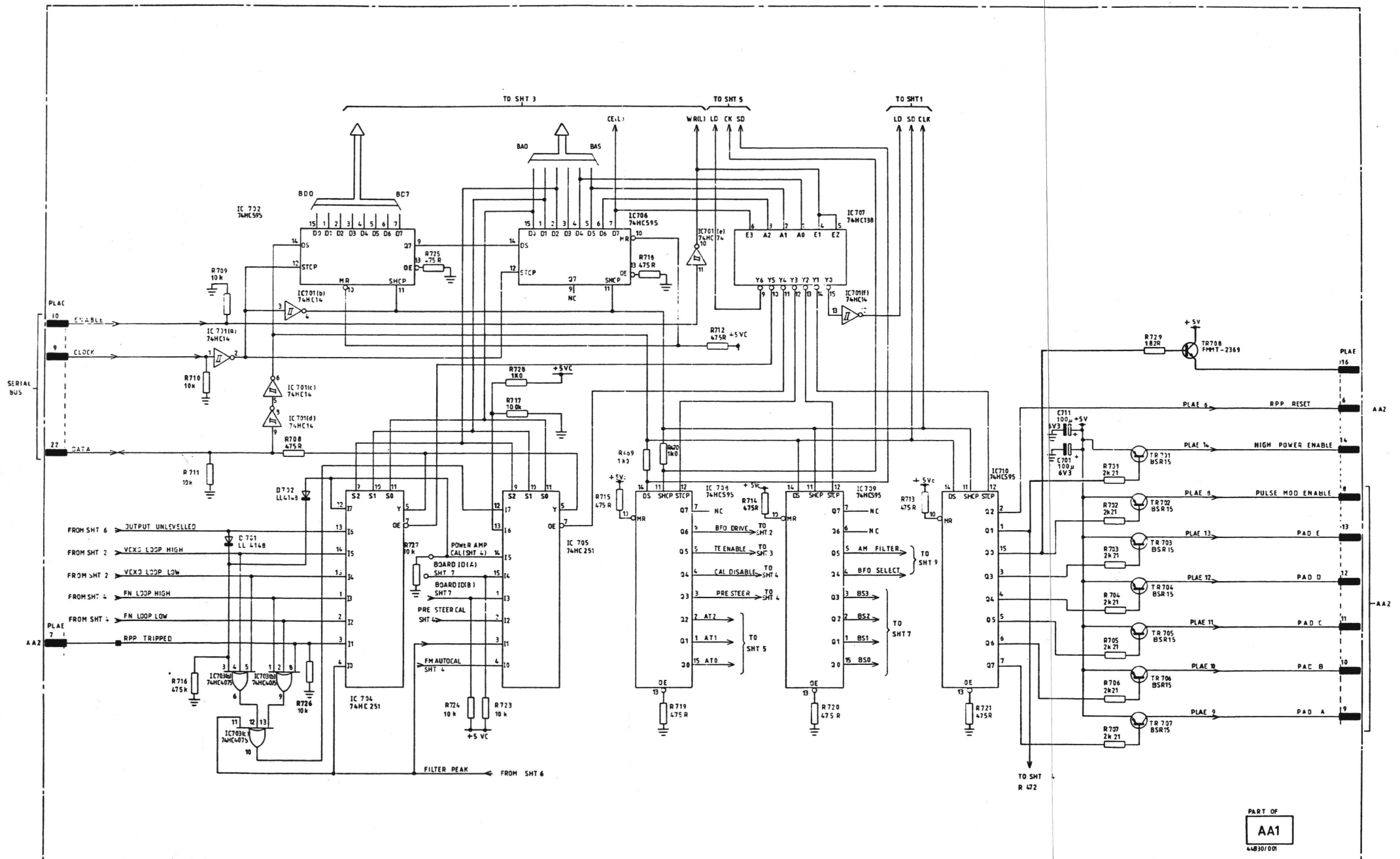
Sheet 8 component locations **AA1**



Frequency generator **AA1**

Fig. 7-18 AA1 RF board: Sheet 8 component locations

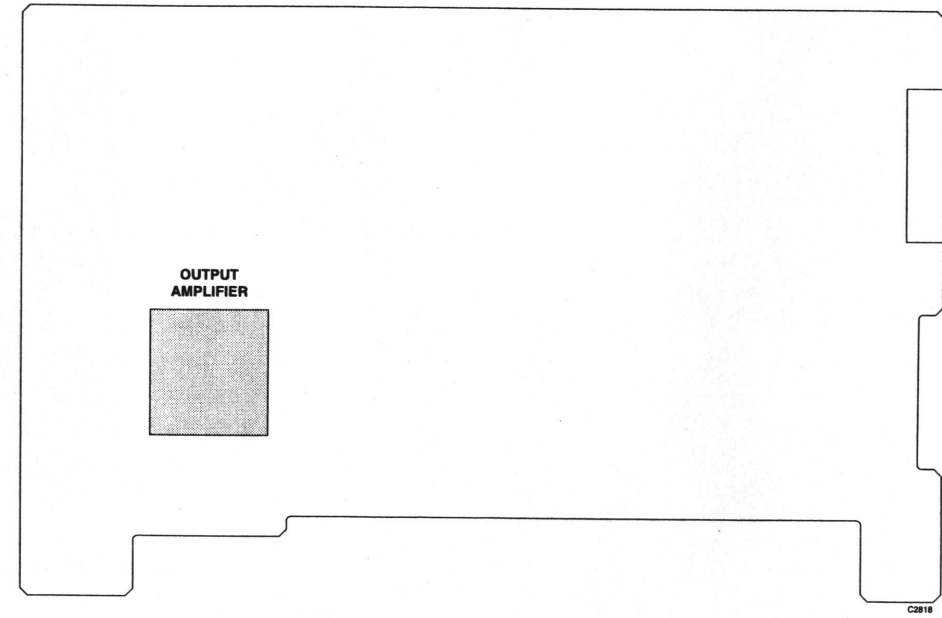
Interface and attenuator drive AA1



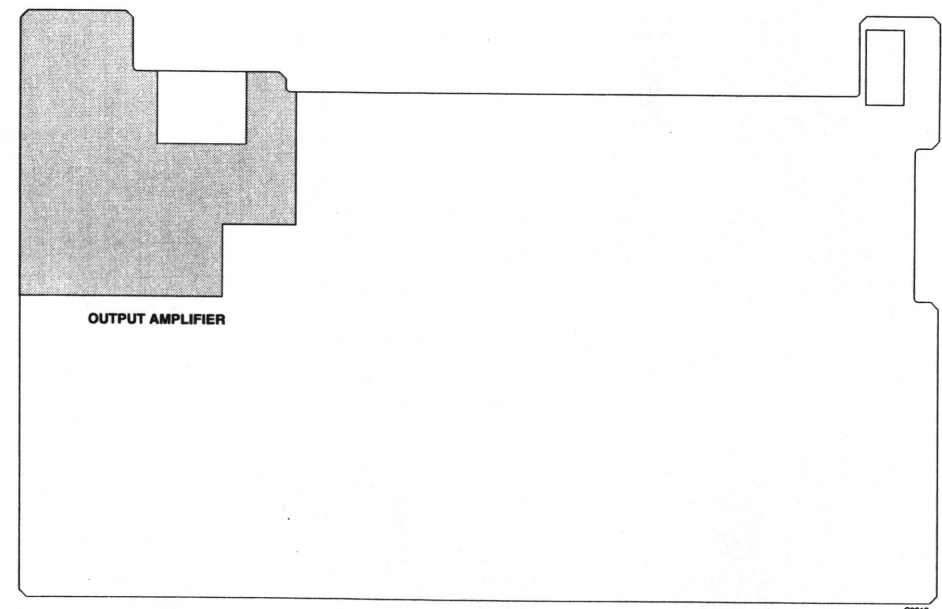
PART OF
AA1
44830/001

Fig. 7-19 AA1 RF board: Interface and attenuator drive circuit

Sheet 9 component locations **AA1**



SOLDER SIDE



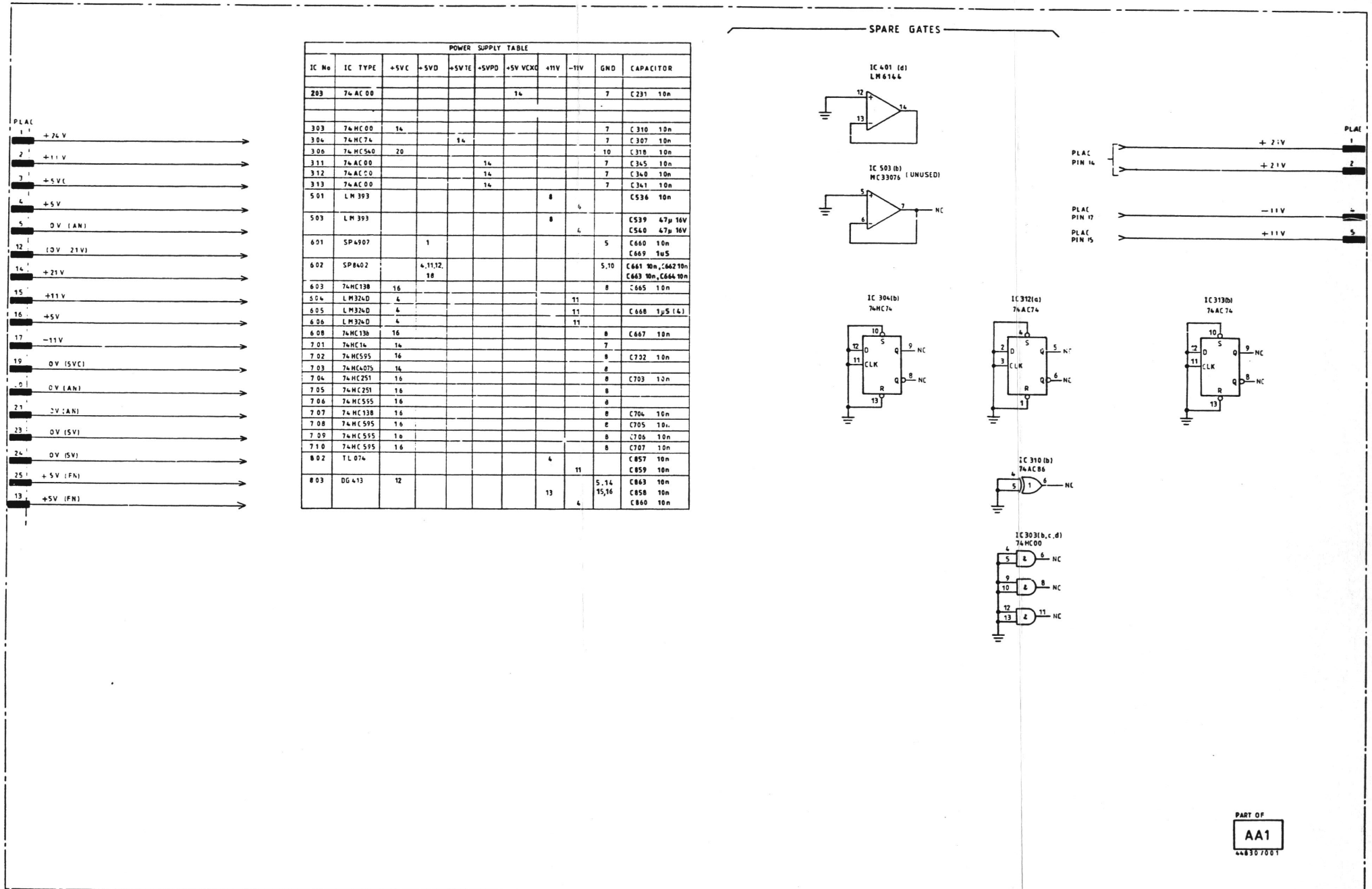
COMPONENT SIDE

Interface and attenuator drive **AA1**

Fig. 7-20 AA1 RF board: Sheet 9 component locations

Output amplifier AA1

Power supplies AA1



Attenuator board AA2

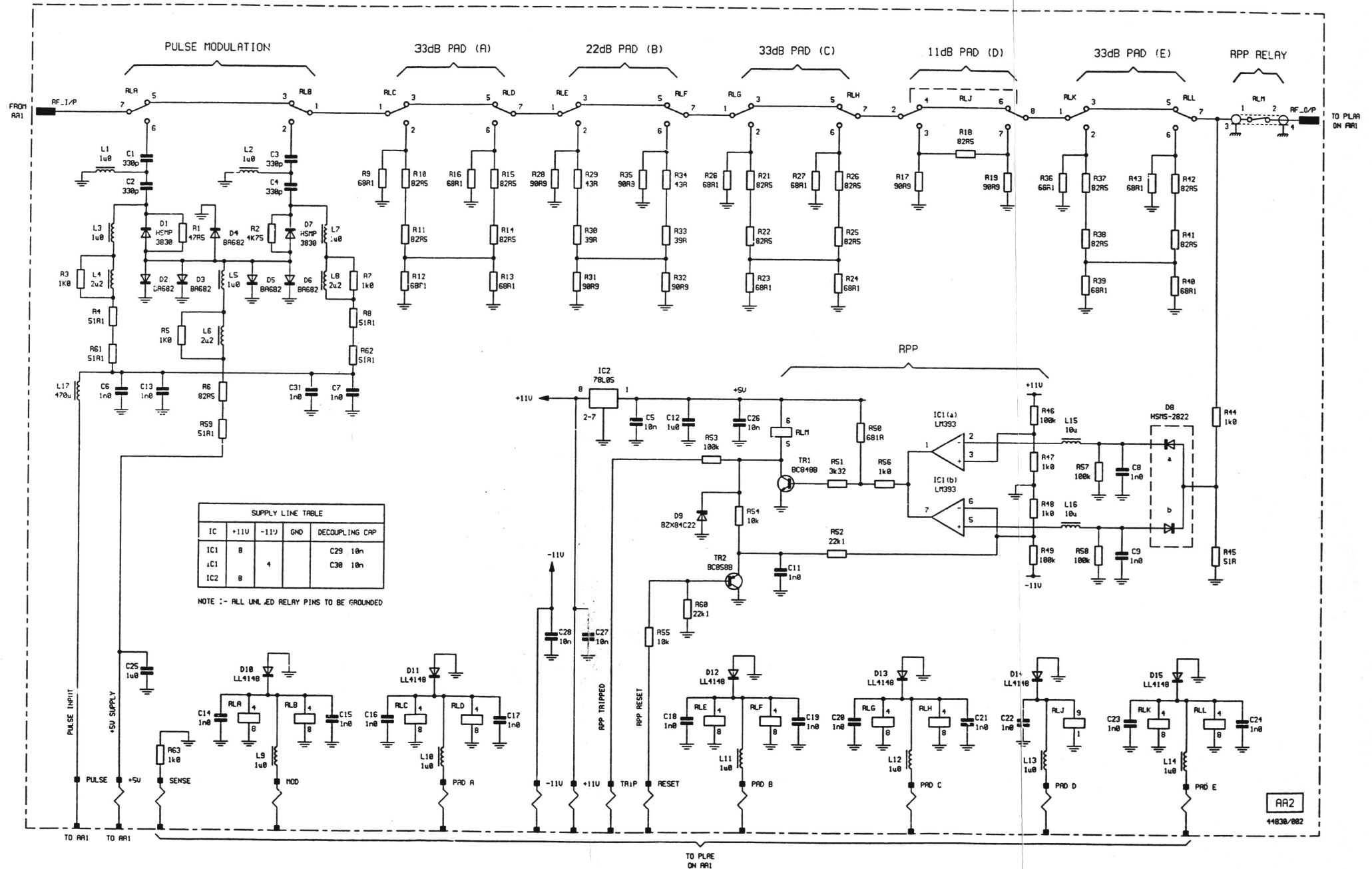
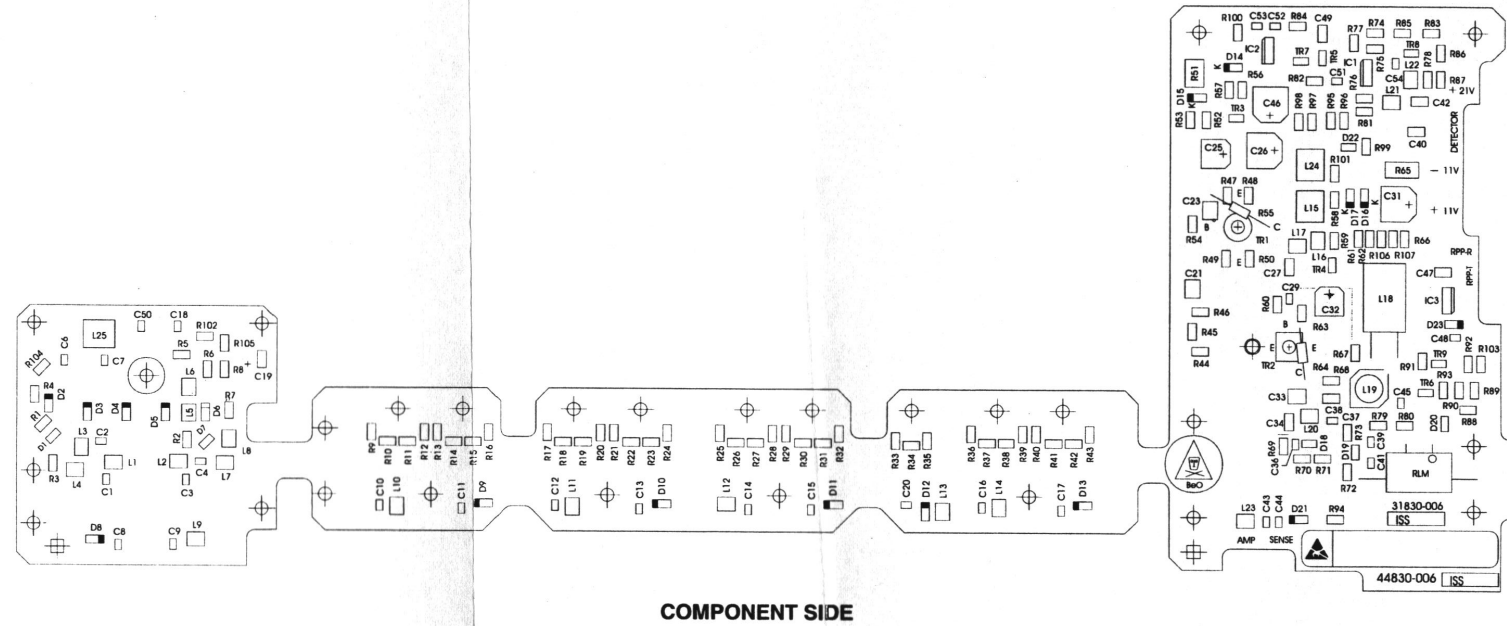


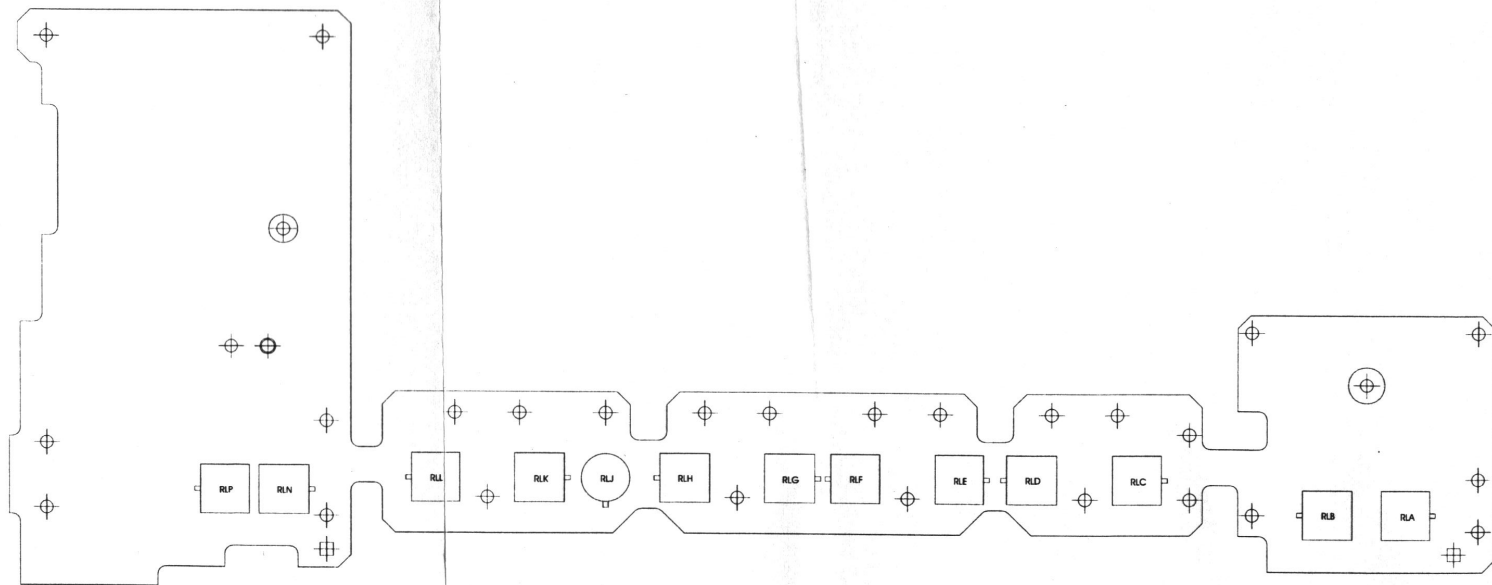
Fig. 7-24 AA2 Attenuator board circuit

Component layout AA2/1



COMPONENT SIDE

Drg. No. E44830/006R Sheet 1 of 2 (Issue 5)



SOLDER SIDE

Attenuator board AA2

Drg. No. E44830/006R Sheet 2 of 2 (Issue 5)

Fig. 7-25 AA2/1 High power attenuator board: Component layouts

Pulse mod and attenuator **AA2/1**

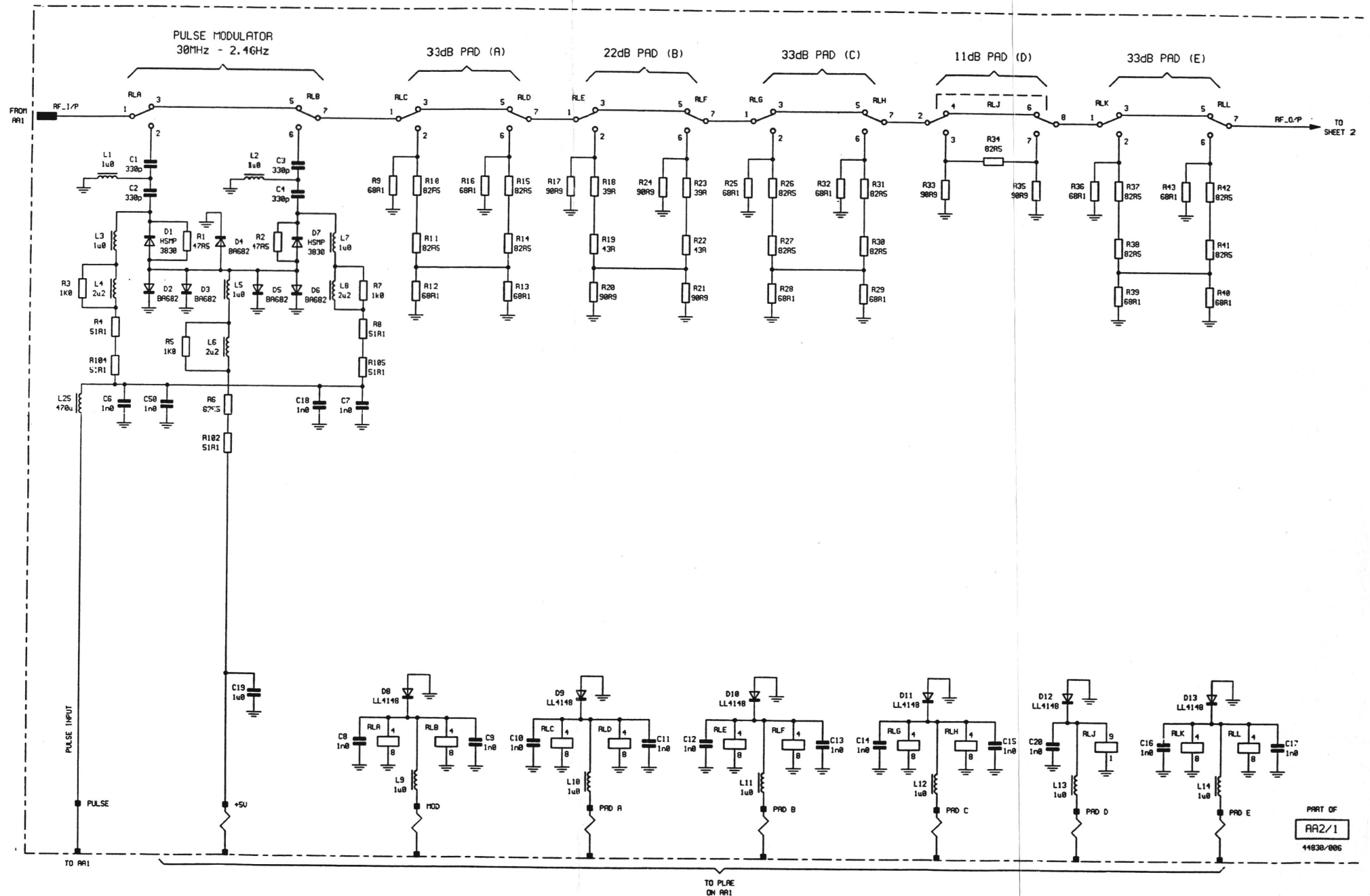
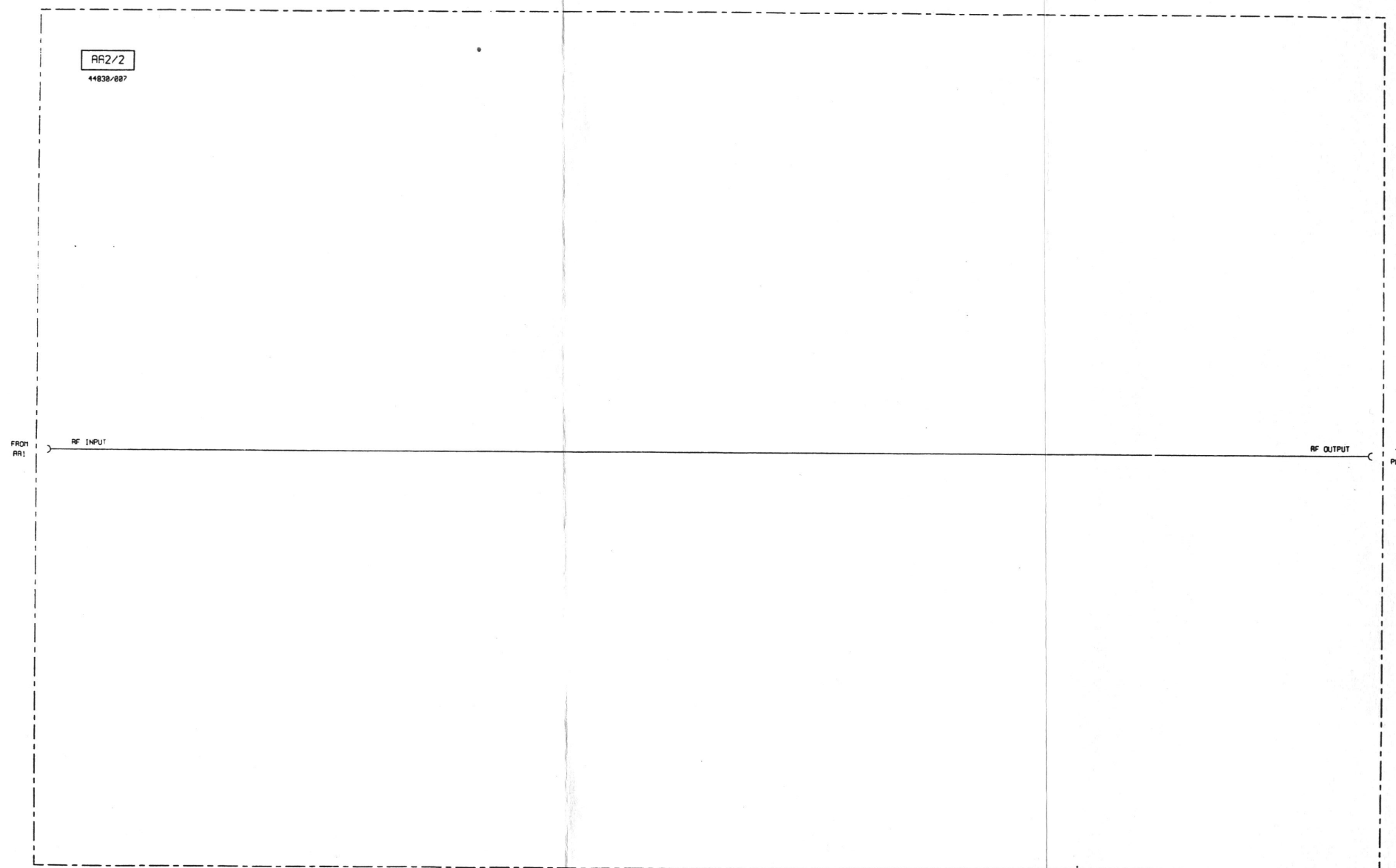


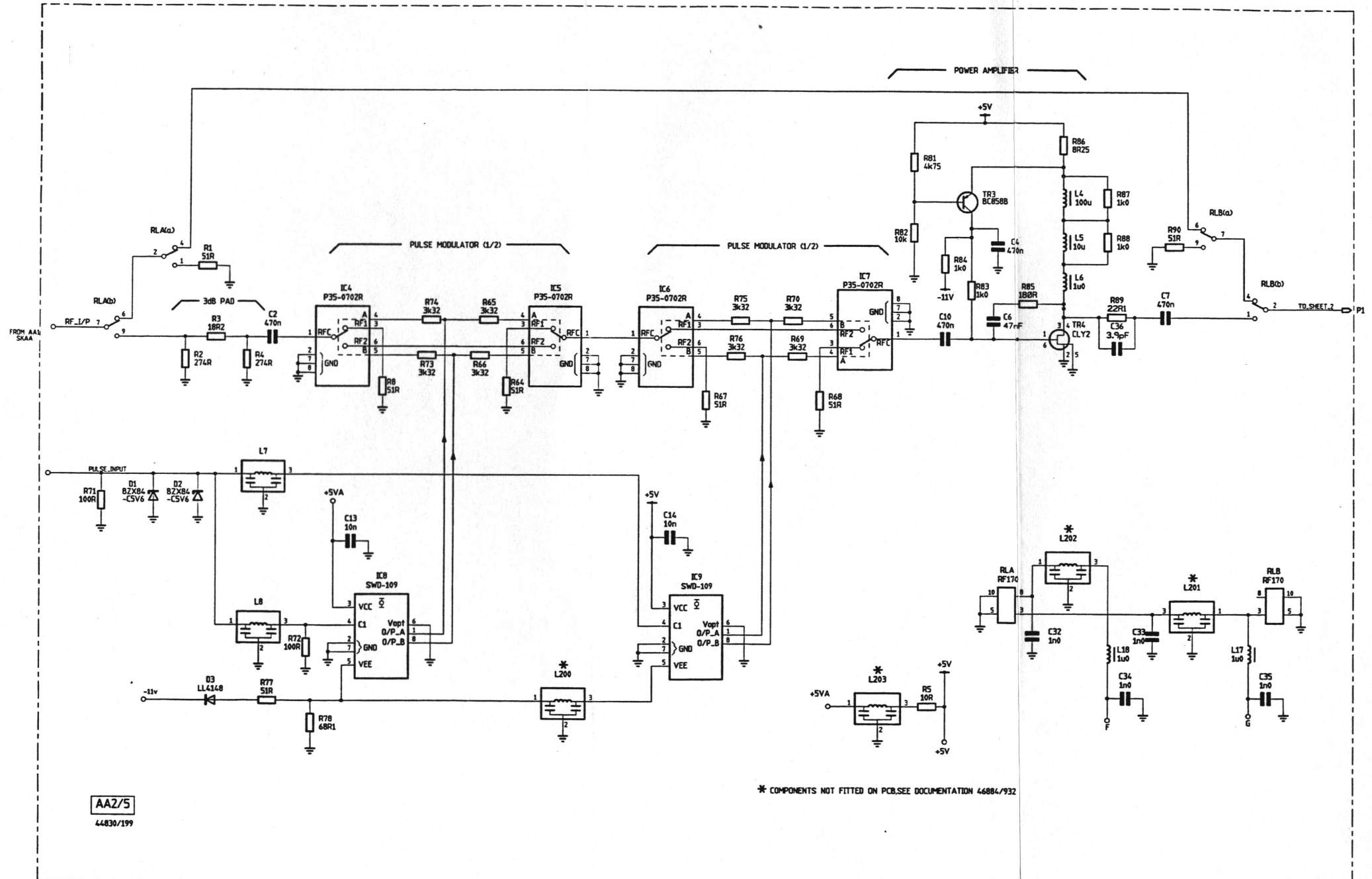
Fig. 7-26 AA2/1 High power attenuator board: Pulse mod and attenuator circuit

Power amp and RPP AA2/1

Signal output **AA2/2**



Pulse mod AA2/5



AA2/5
44830/199

Fig. 7-30 AA2/5 Fast pulse modulator board: Pulse mod circuit

Pulse mod AA2/5

RPP and atten AA2/5

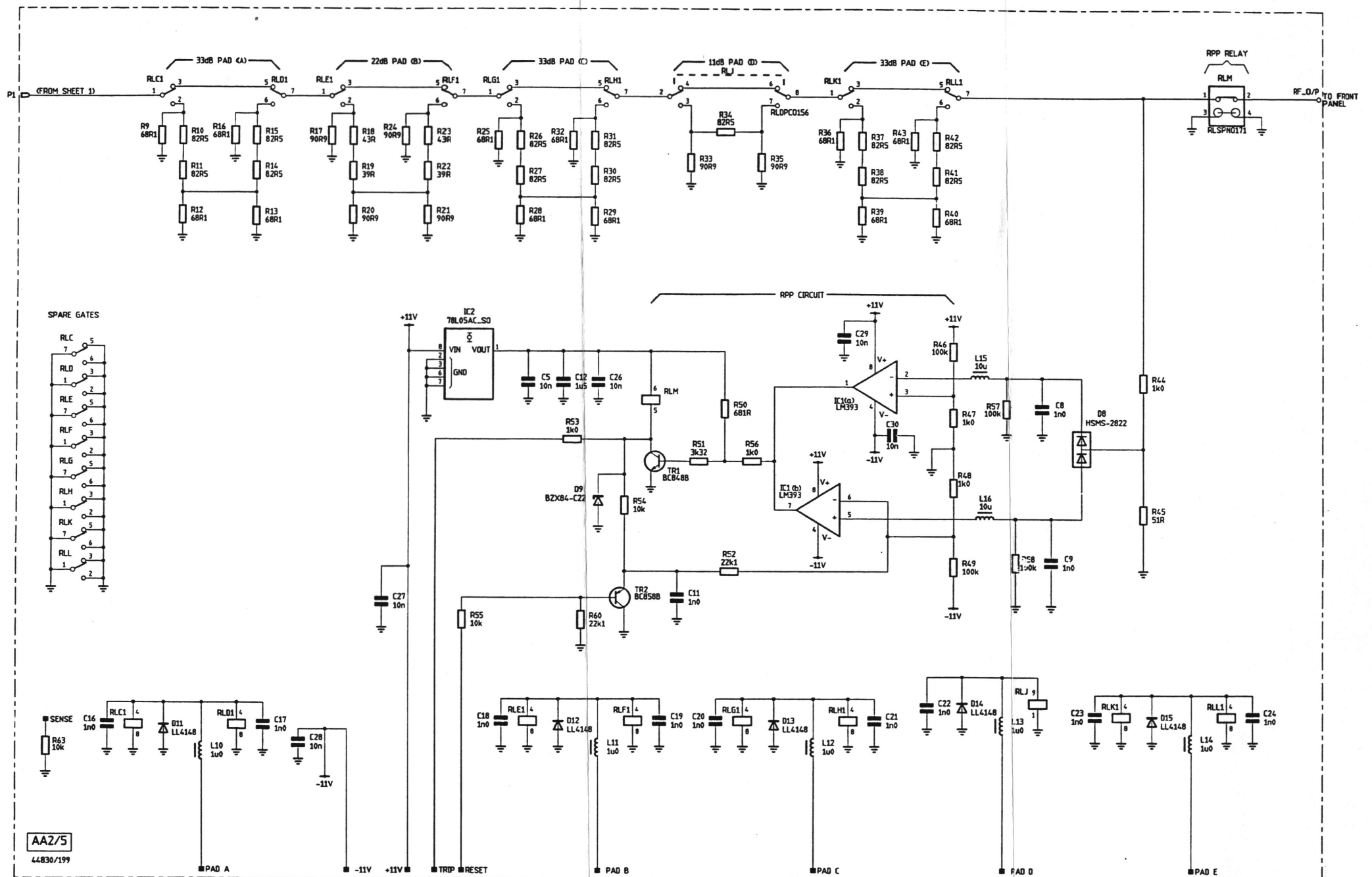
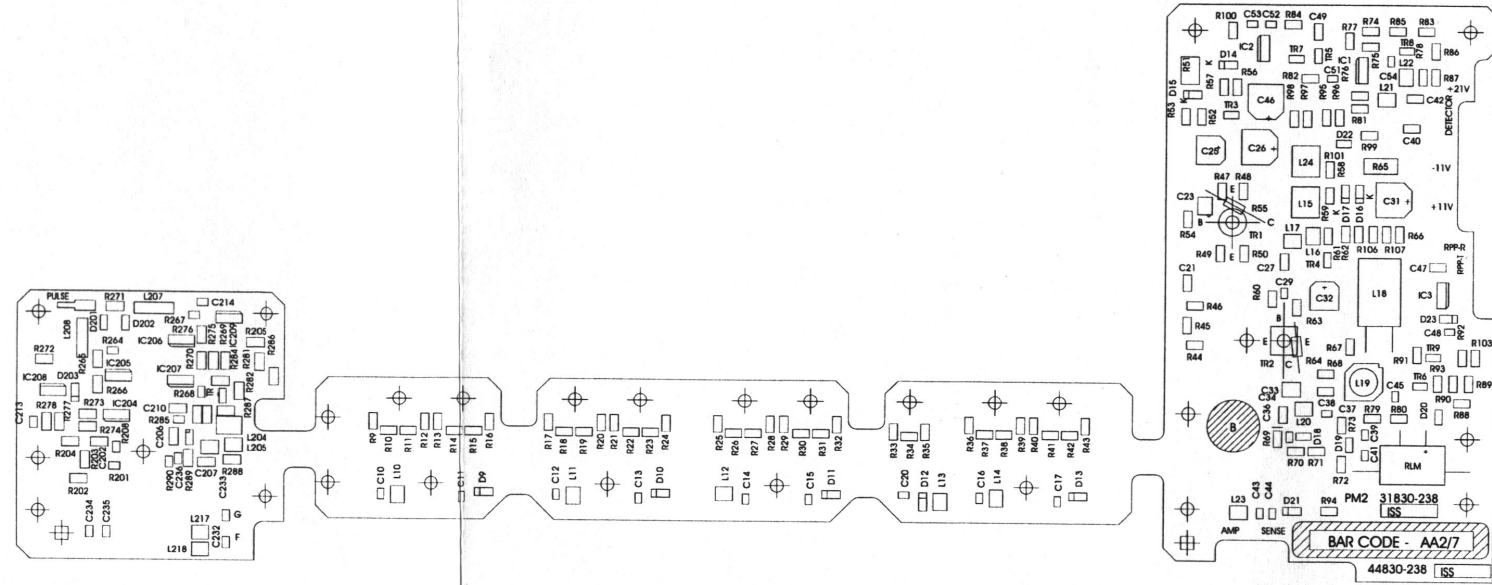


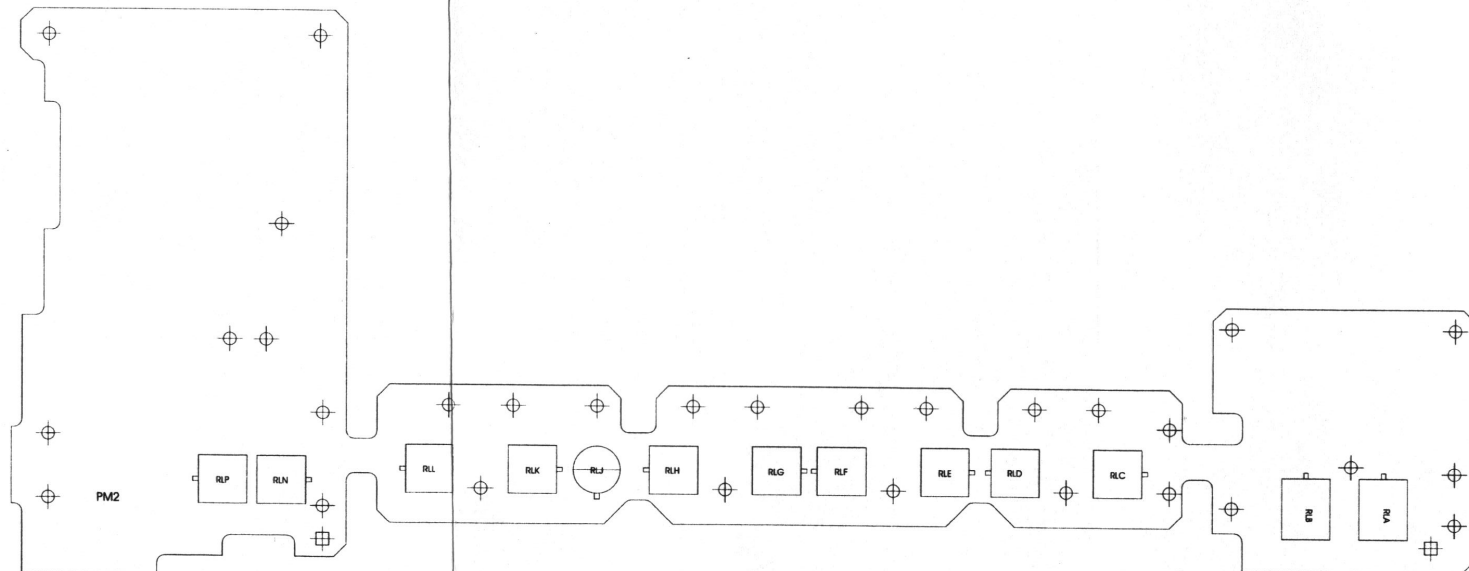
Fig. 7-31 AA2/5 Fast pulse modulator board: RPP and atten circuit

Component layout **AA2/7**



COMPONENT SIDE

Drg. No. E44830/238P Sheet 1 of 2 (Issue 1)



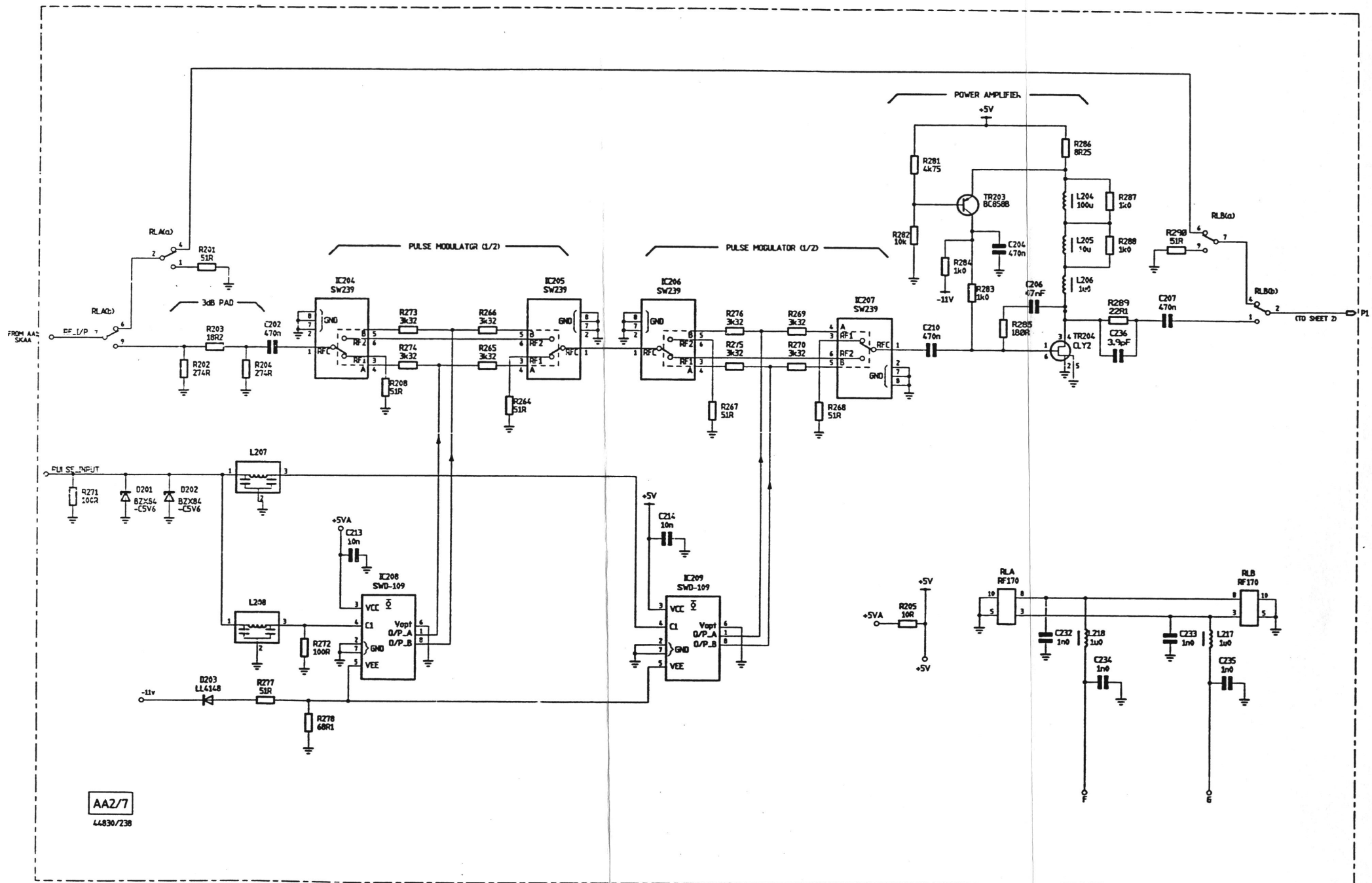
SOLDER SIDE

RPP and atten **AA2/5**

Drg. No. E44830/238P Sheet 2 of 2 (Issue 1)

Fig. 7-32 AA2/7 Fast pulse and high power board: Component layouts

Pulse mod AA2/7

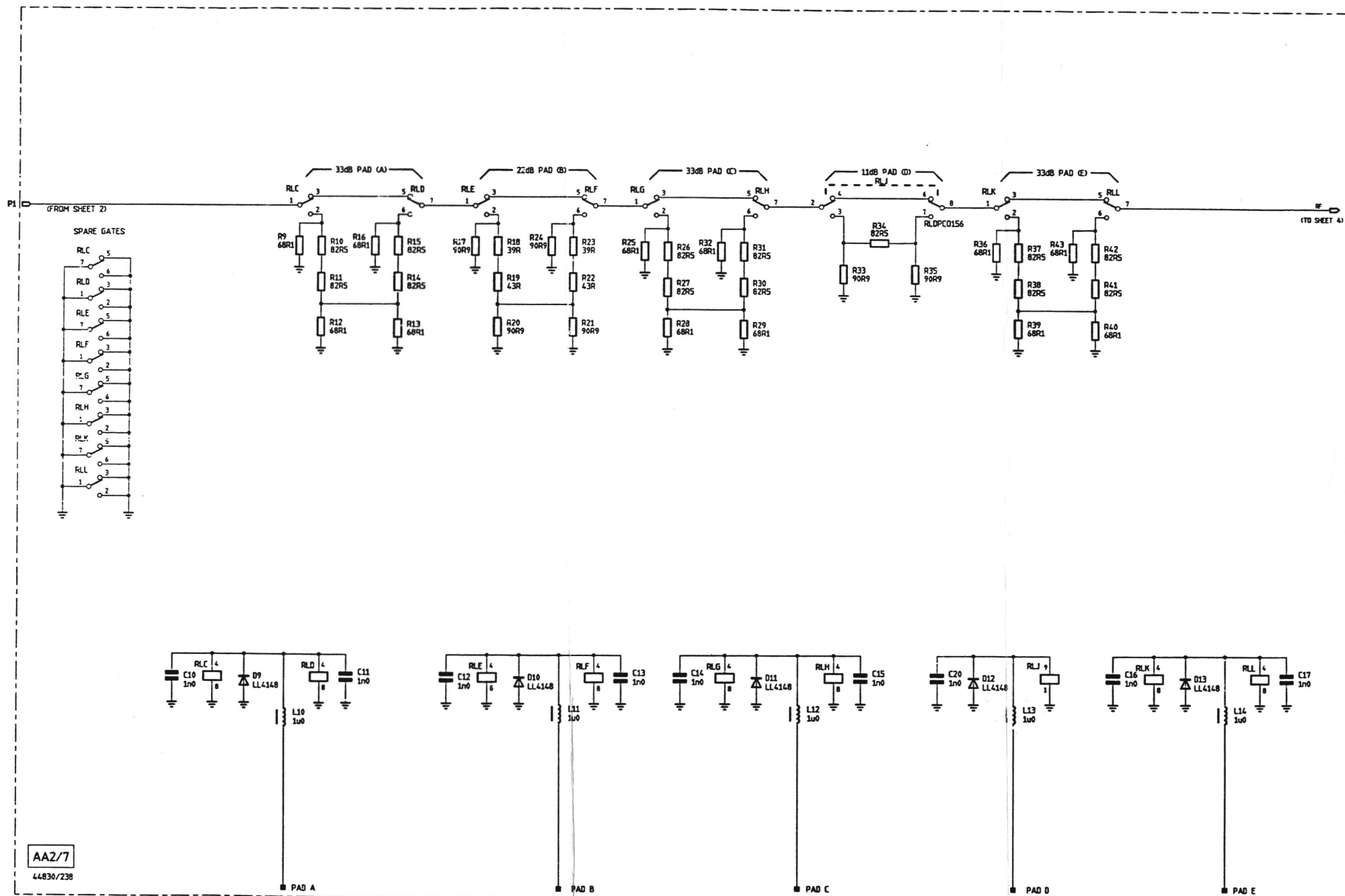


AA2/7
44830/238

Fig. 7-33 AA2/7 Fast pulse and high power board: Pulse mod circuit

Pulse mod AA2/7

Attenuator AA2/7



Attenuator AA2/7

Power amp and RPP AA2/7

Component layout AB1

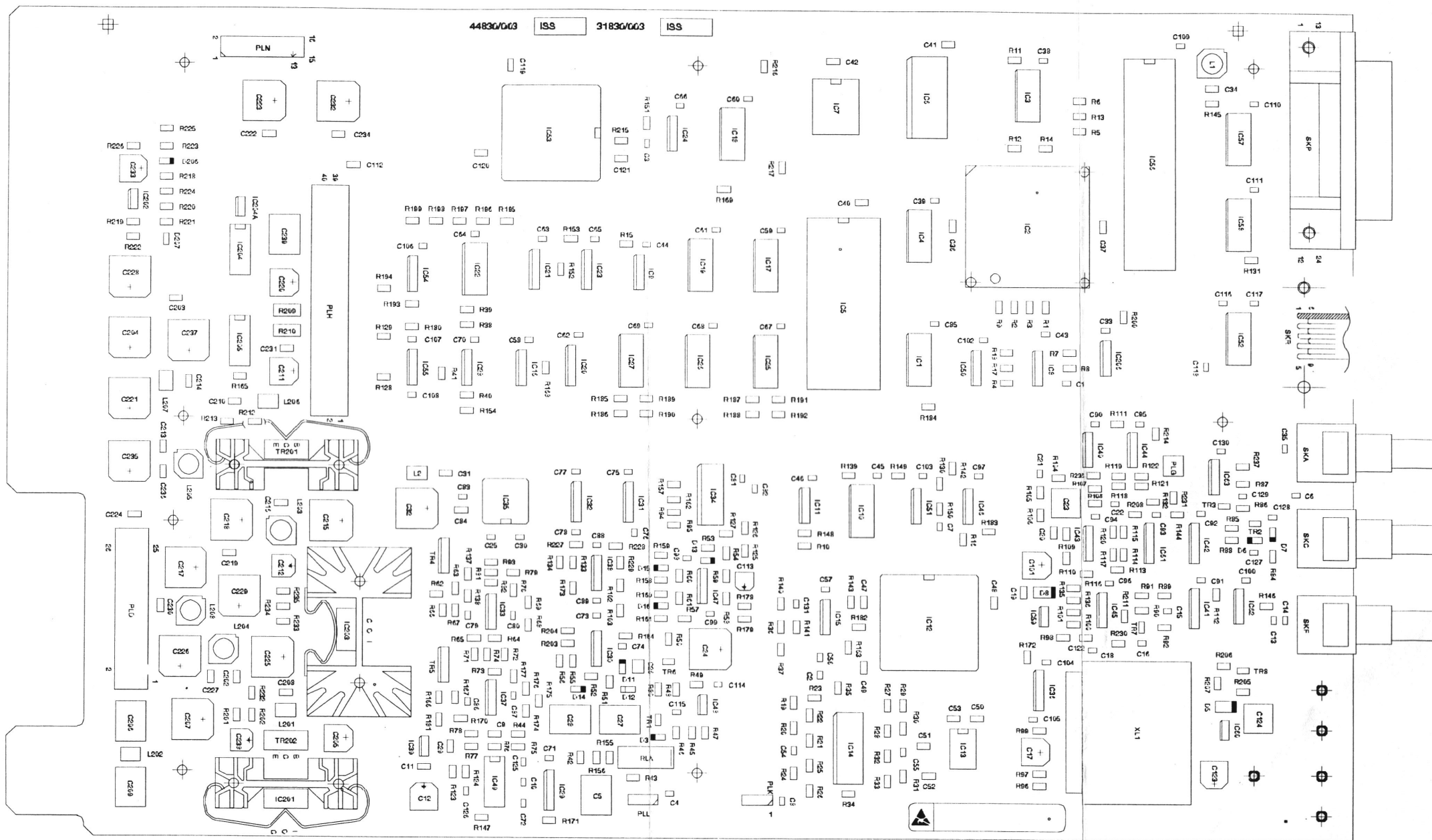
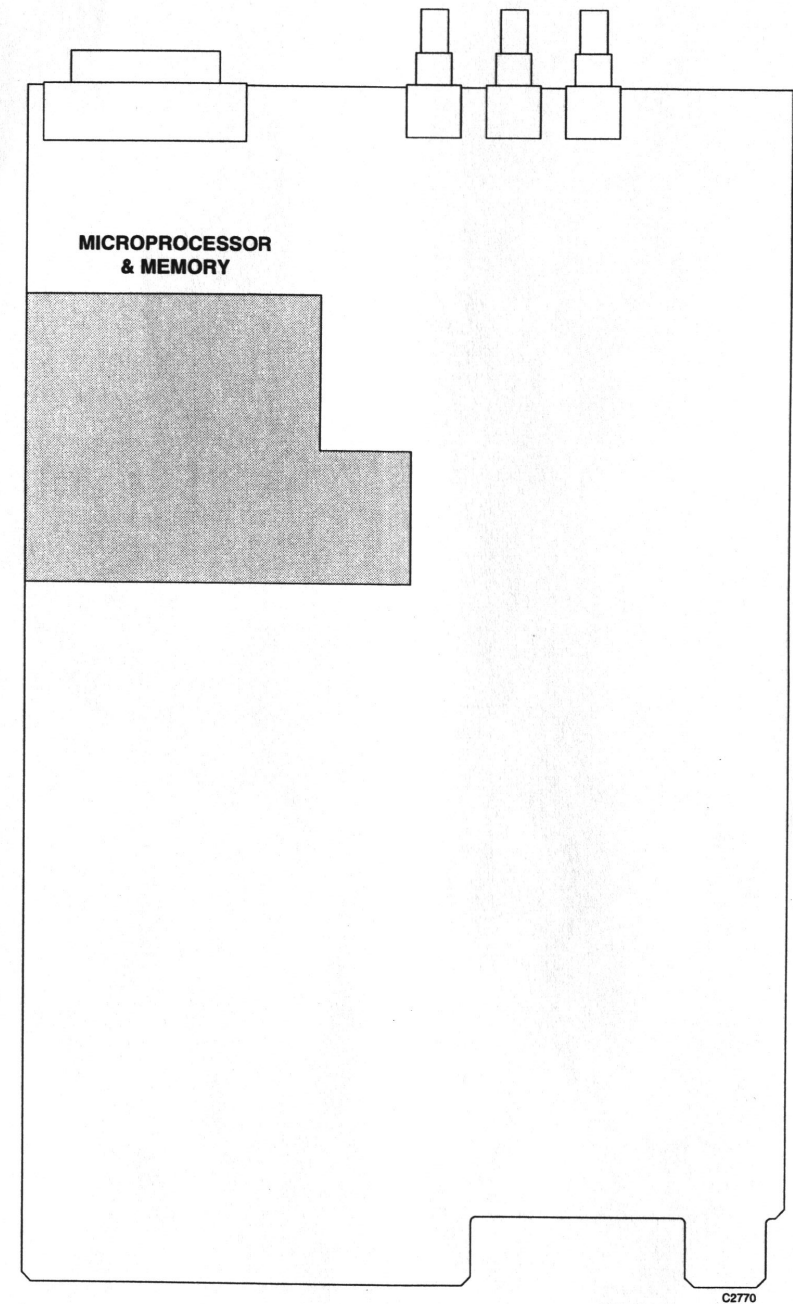


Fig. 7-36 AB1 Control board: Component layout

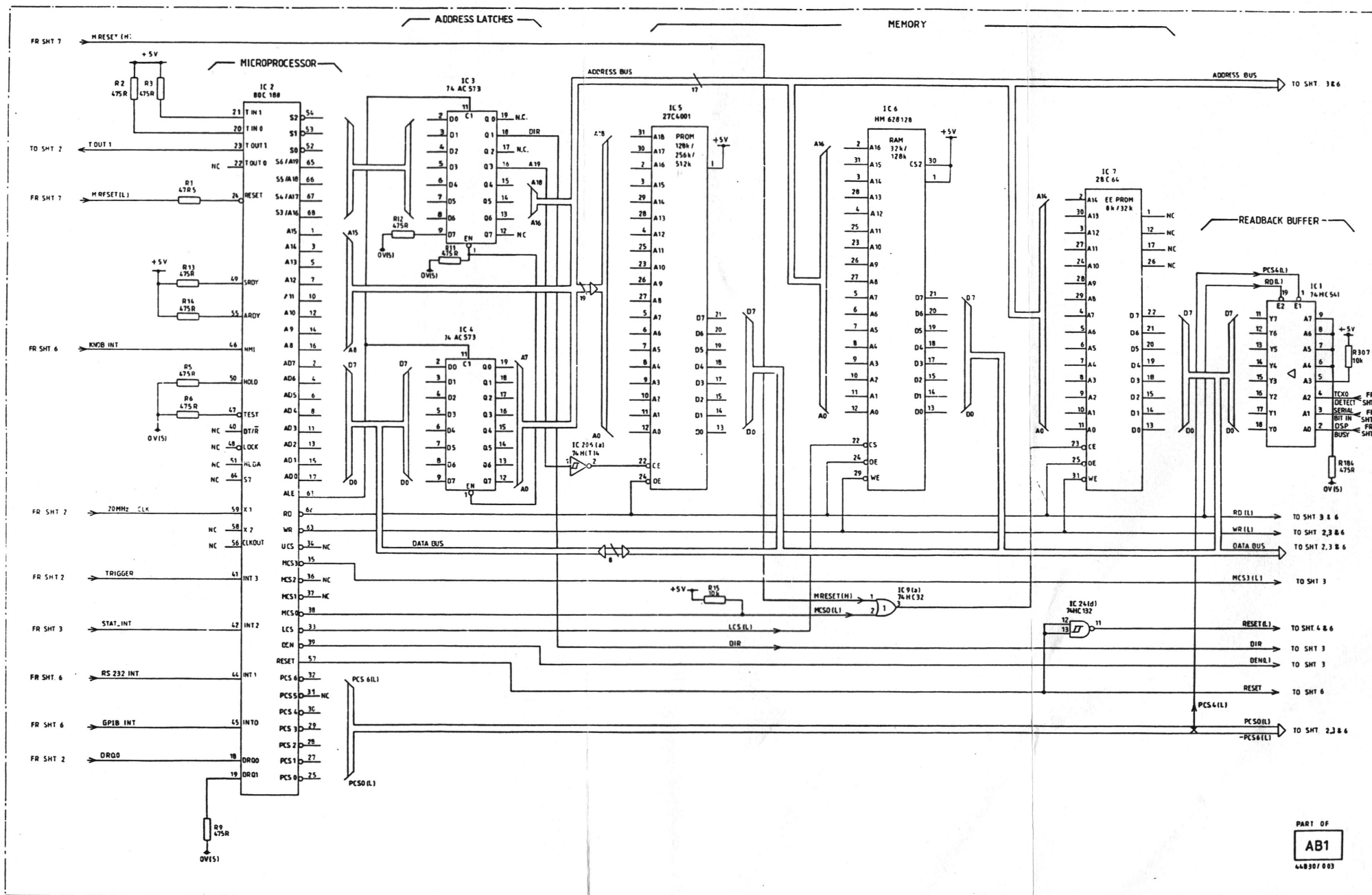
Sheet 1 component locations **AB1**



Component layout **AB1**

Fig. 7-37 AB1 Control board: Sheet 1 component locations

Microprocessor and memory AB1



PART OF
AB1
44830/003

Fig. 7-38 AB1 Control board: Microprocessor and memory circuit

Sheet 2 component locations **AB1**

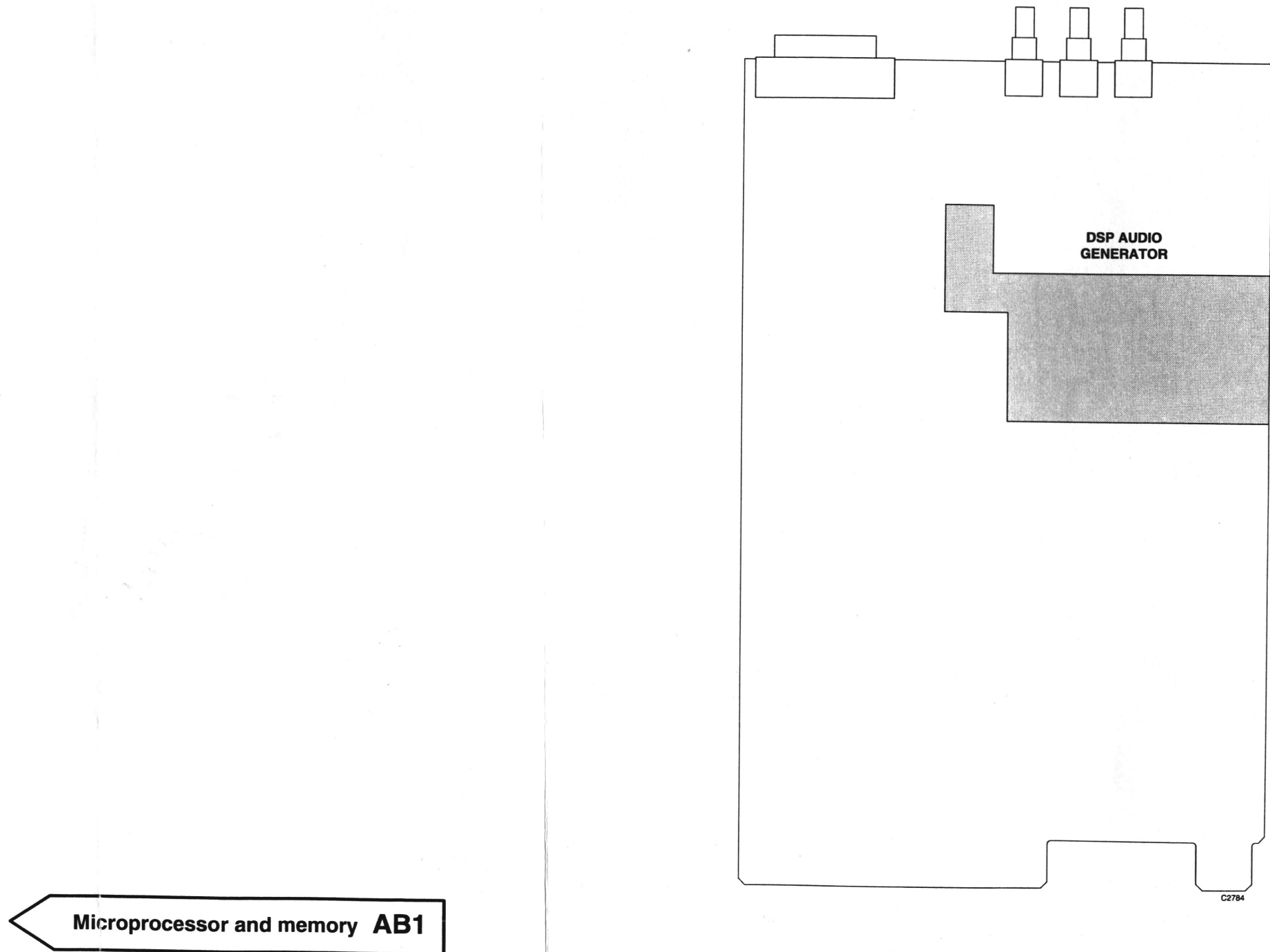


Fig. 7-39 AB1 Control board: Sheet 2 component locations

DSP audio generator AB1

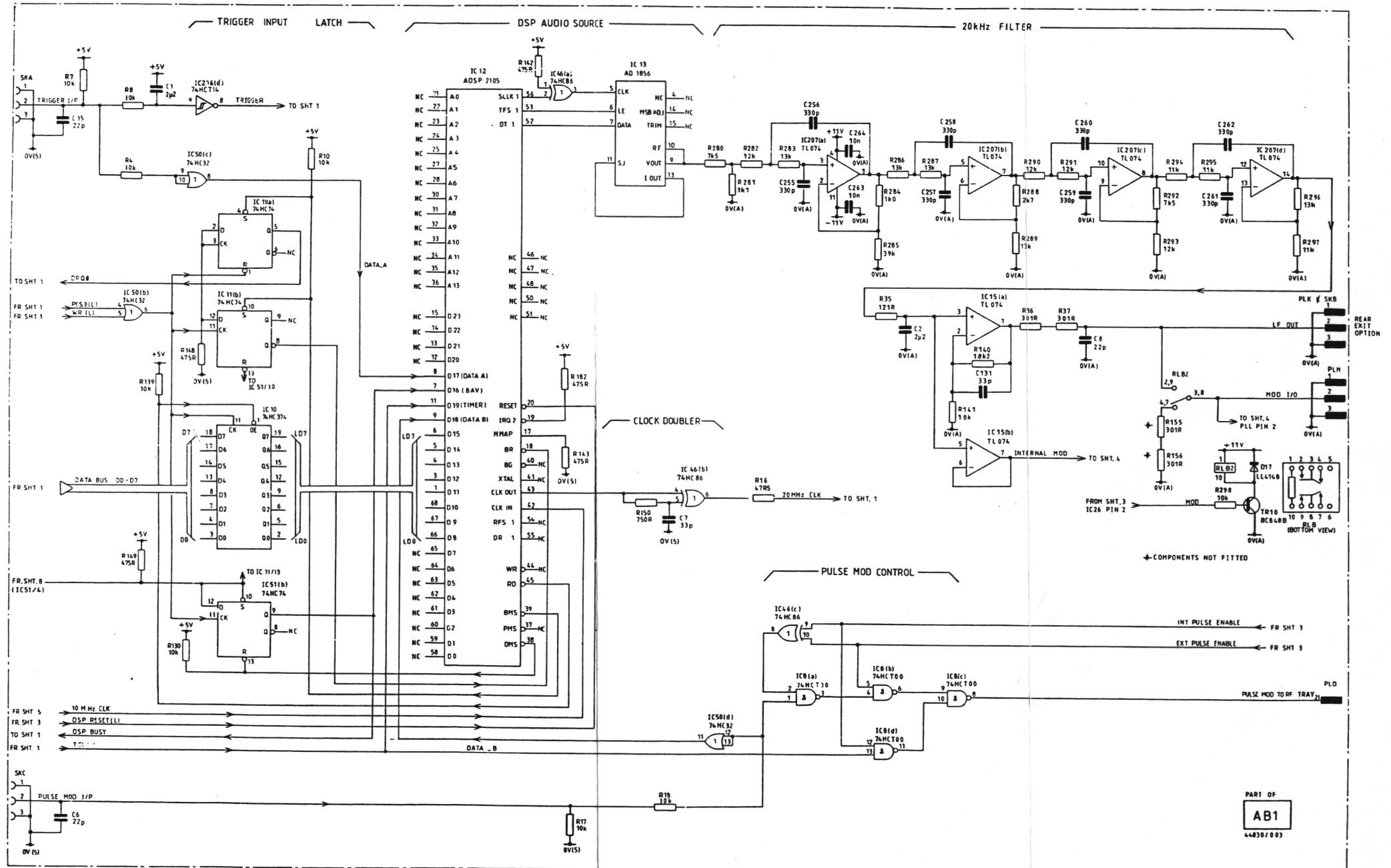


Fig. 7-40 AB1 Control board: DSP audio generator circuit

Sheet 3 component locations **AB1**

DSP audio generator **AB1**

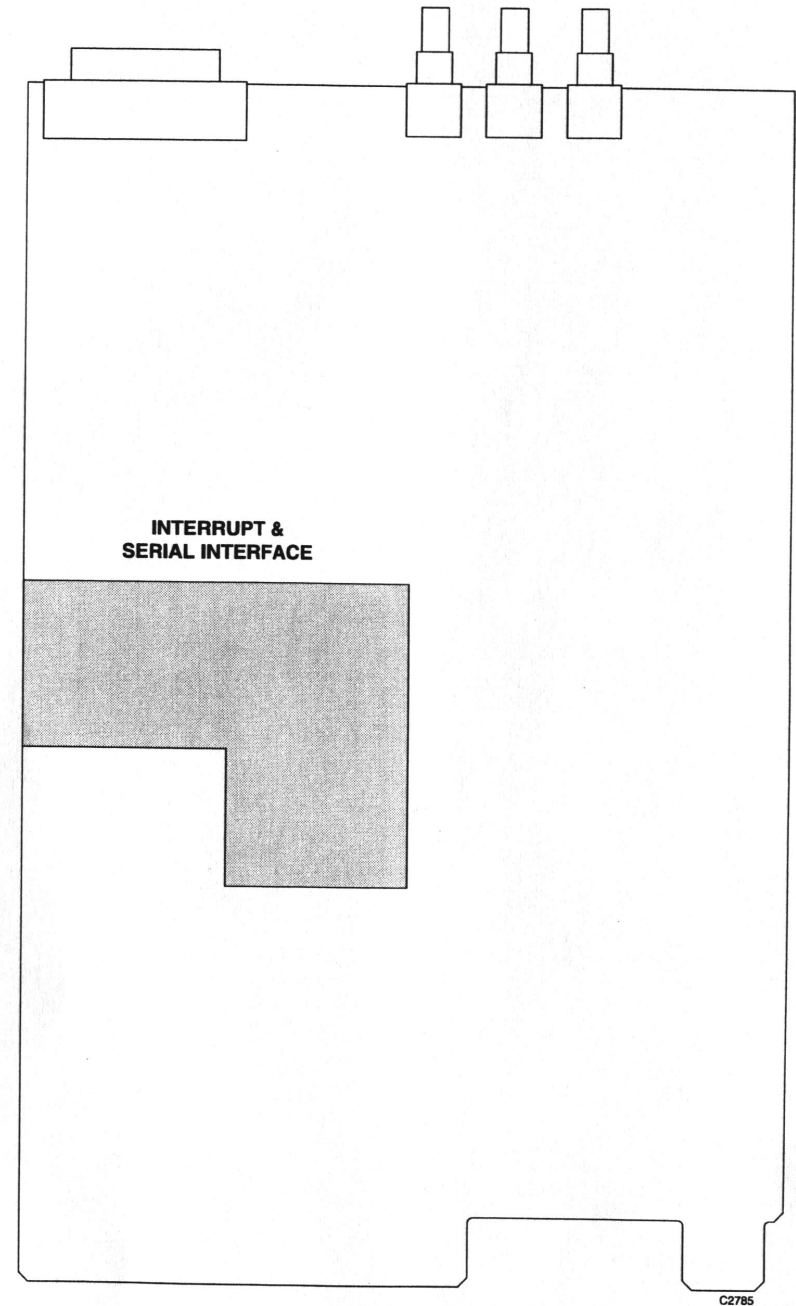


Fig. 7-41 AB1 Control board: Sheet 3 component locations

Interrupts and serial interface AB1

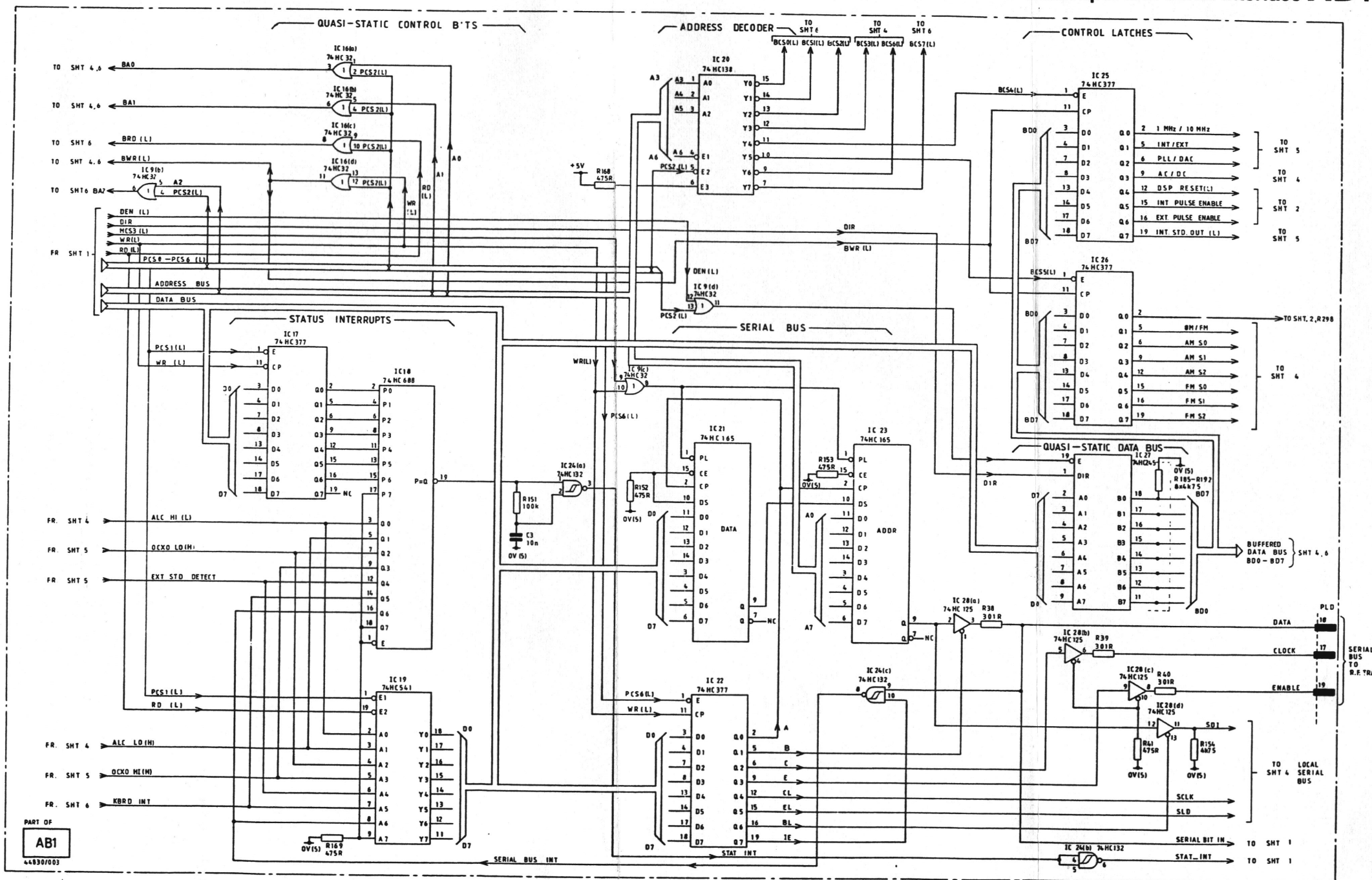
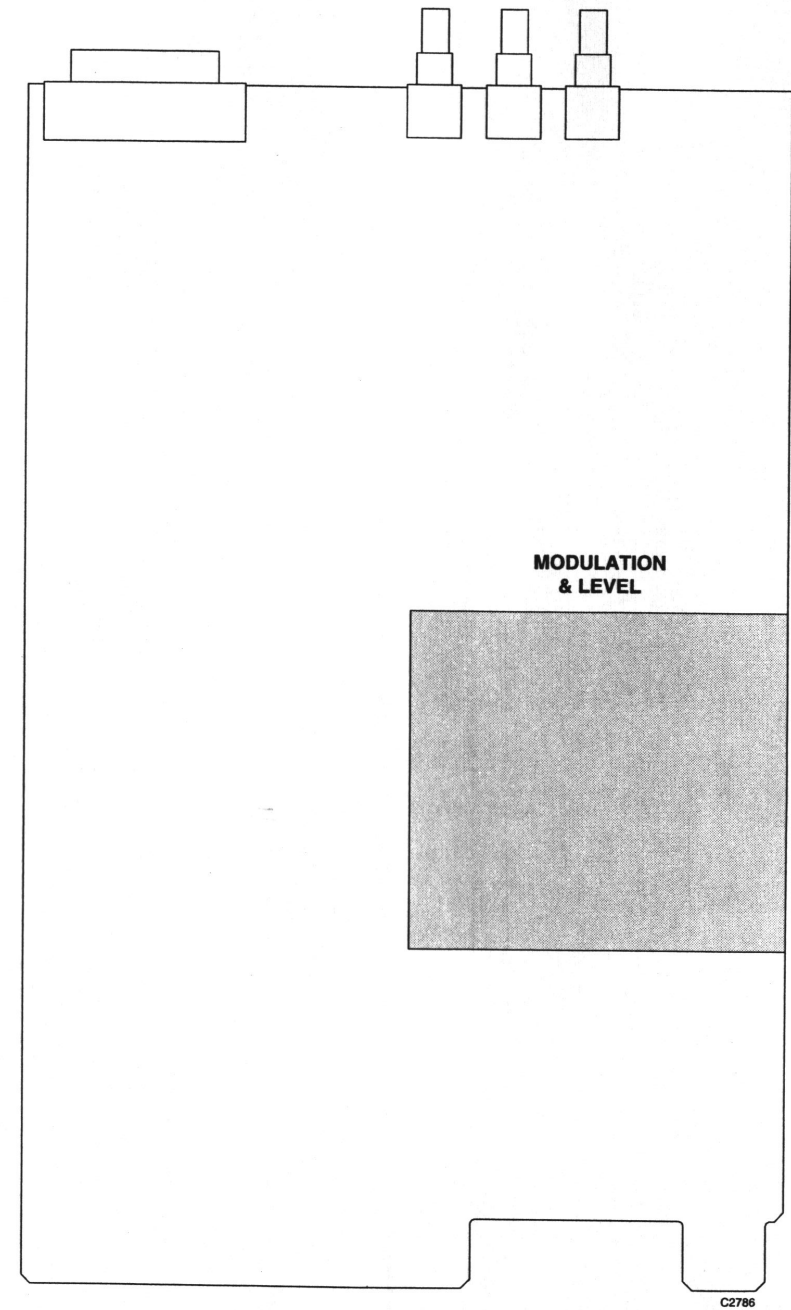


Fig. 7-42 AB1 Control board: Interrupts and serial interface circuit

Sheet 4 component locations **AB1**



Interrupts and serial interface **AB1**

Fig. 7-43 AB1 Control board: Sheet 4 component locations

Modulation and level AB1

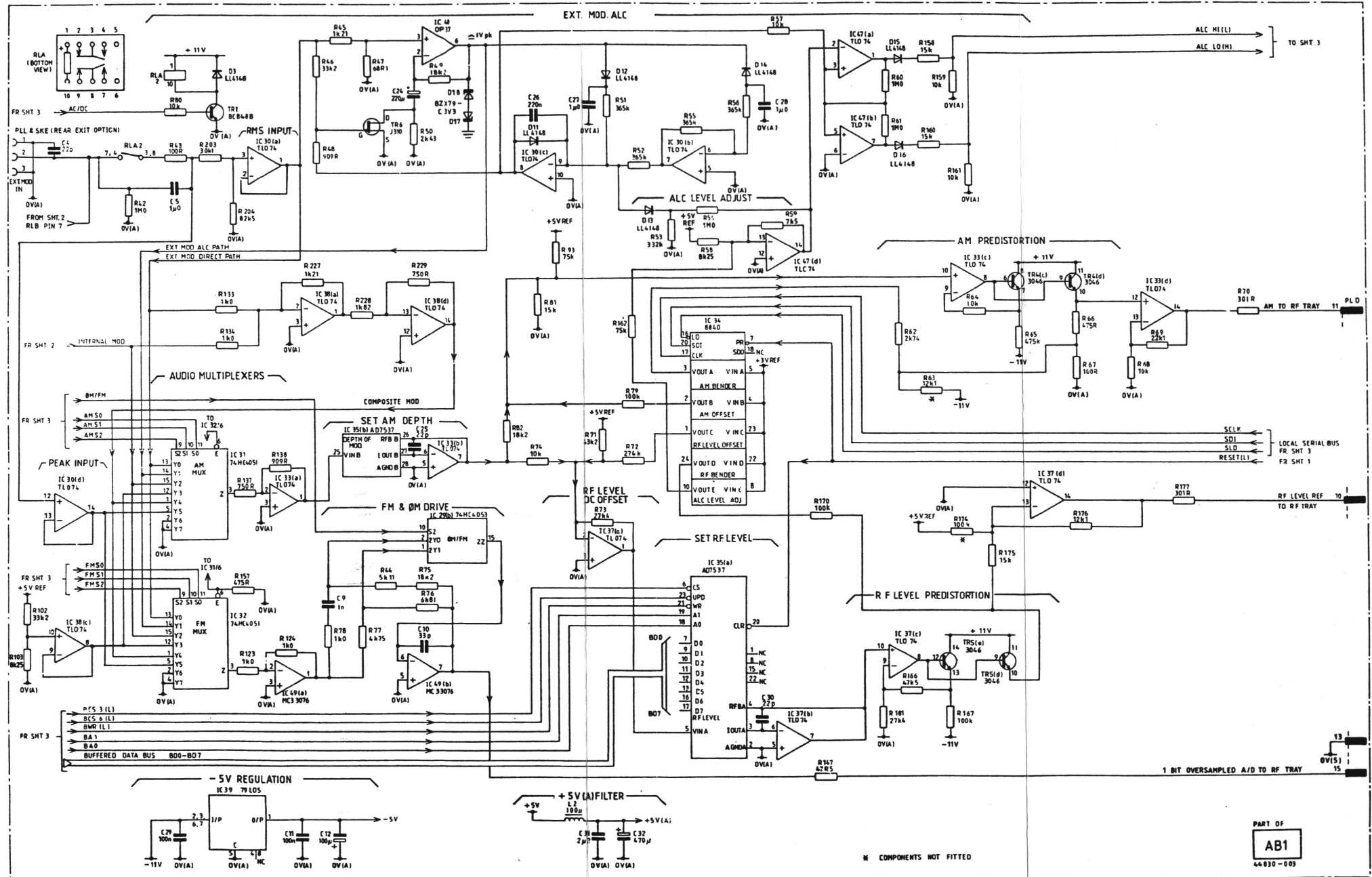
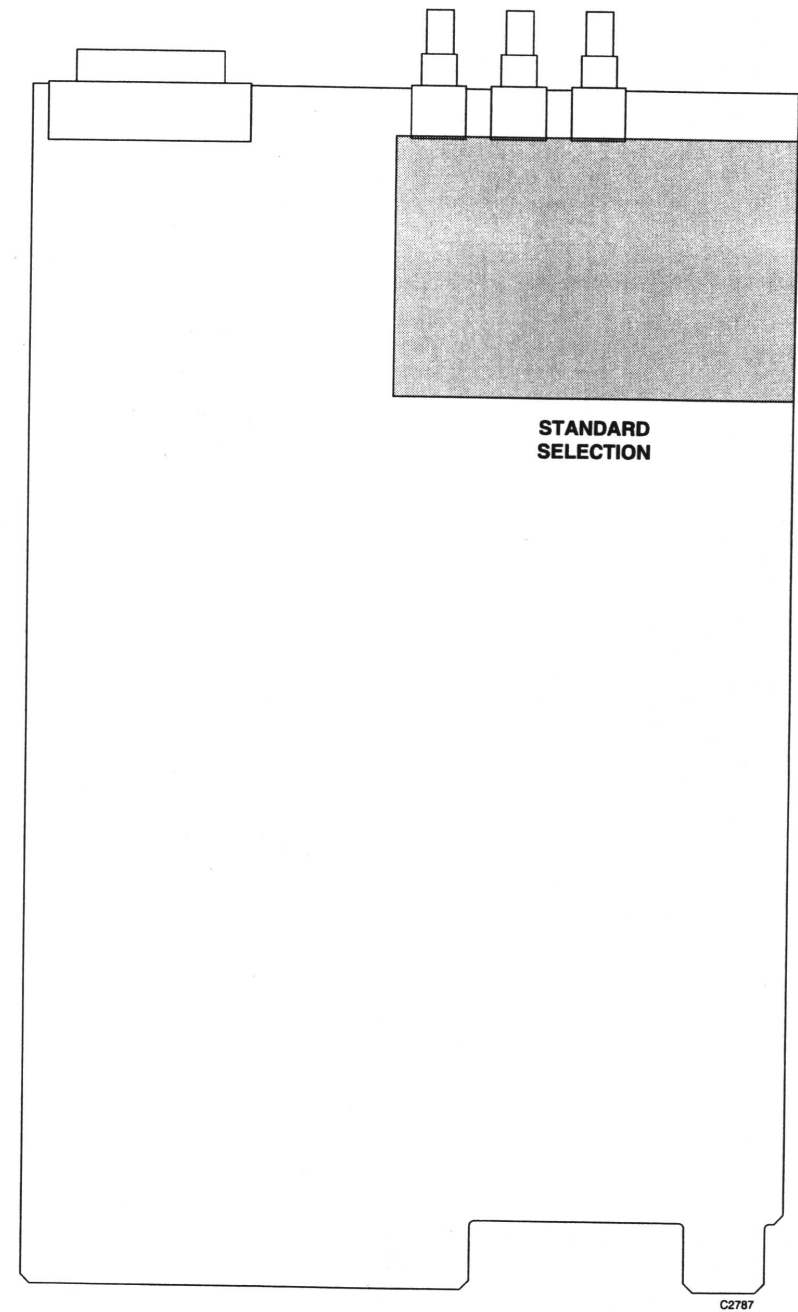


Fig. 7-44 AB1 Control board: Modulation and level circuit

Sheet 5 component locations **AB1**



Modulation and level **AB1**

Fig. 7-45 AB1 Control board: Sheet 5 component locations

Standard selection AB1

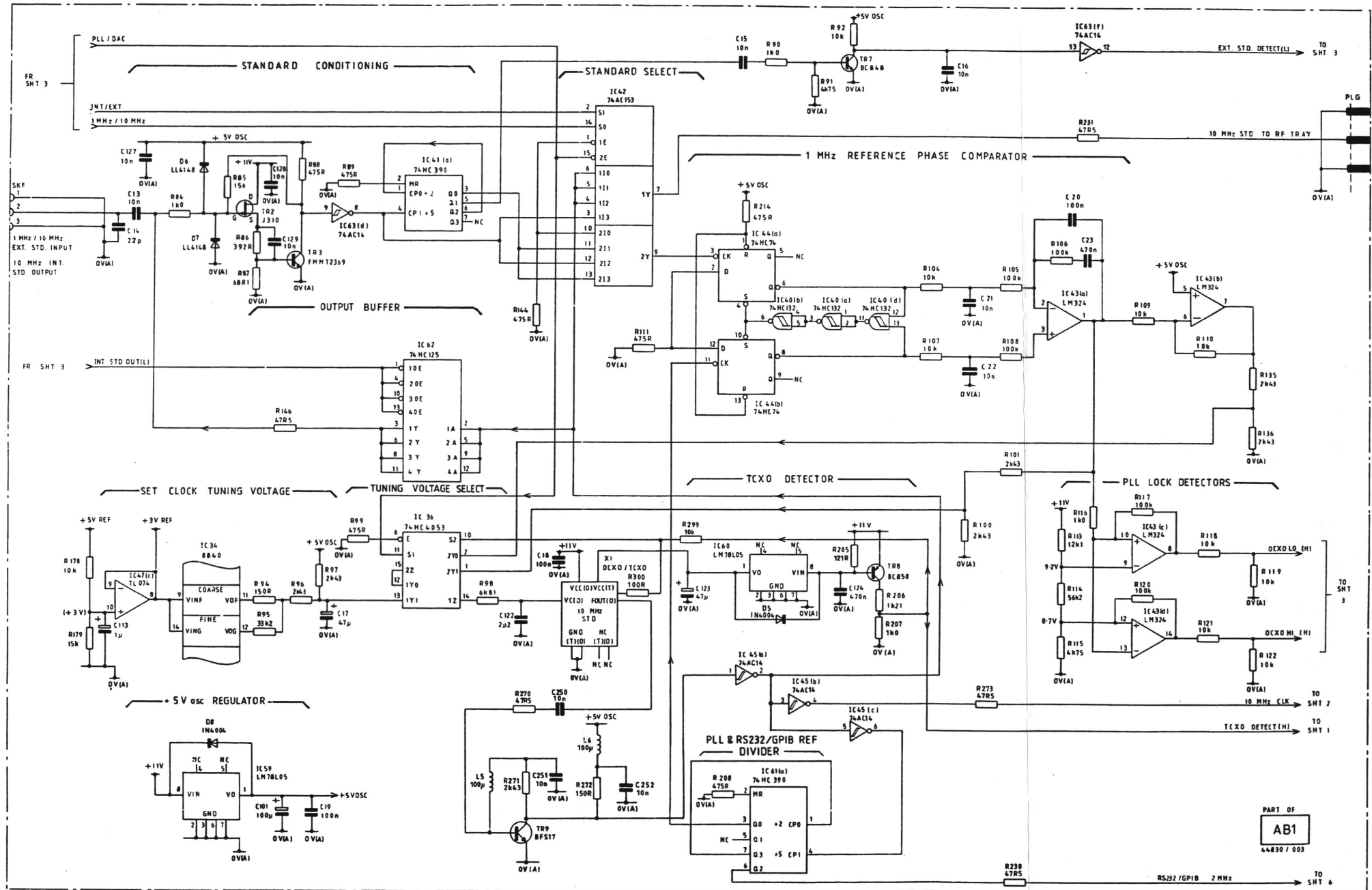
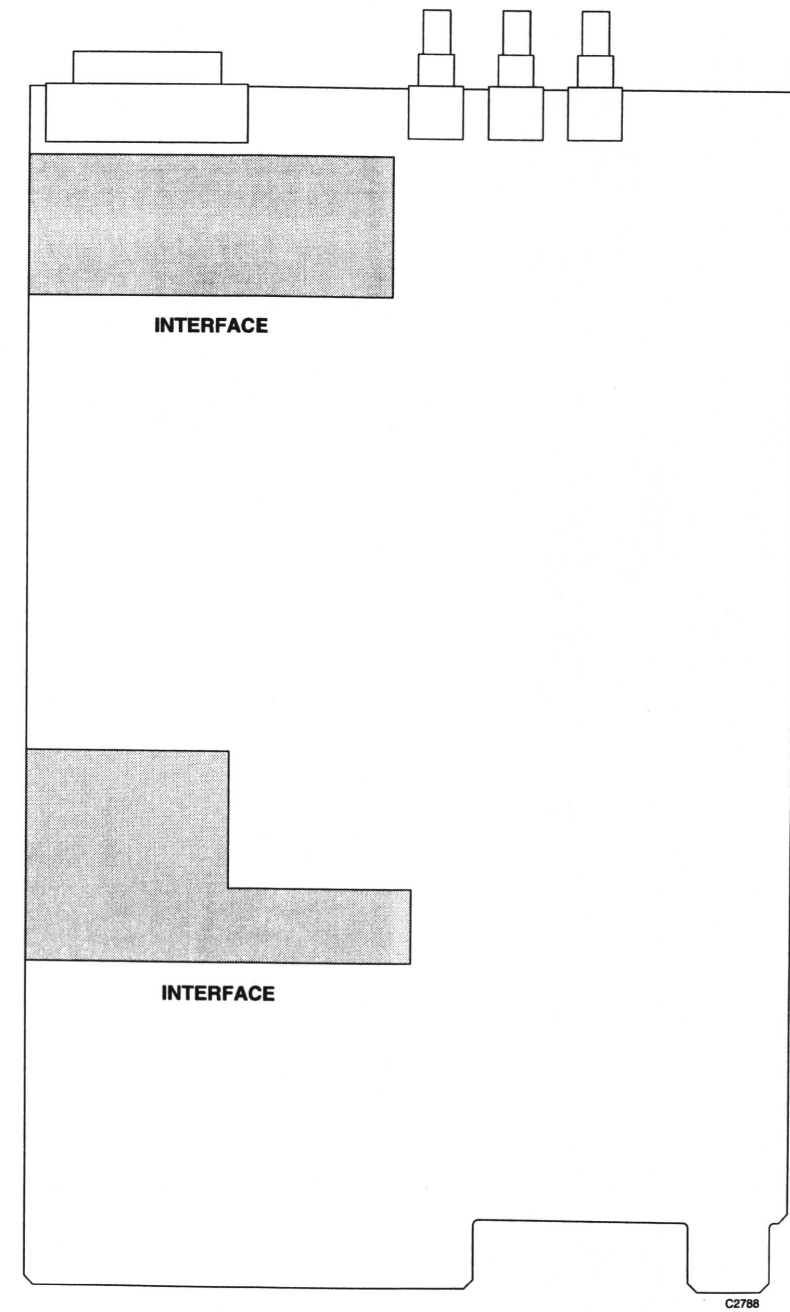


Fig. 7-46 AB1 Control board: Standard selection circuit

Sheet 6 component locations **AB1**



Standard selection **AB1**

Fig. 7-47 AB1 Control board: Sheet 6 component locations

Sheet 7 component locations **AB1**

Interface **AB1**

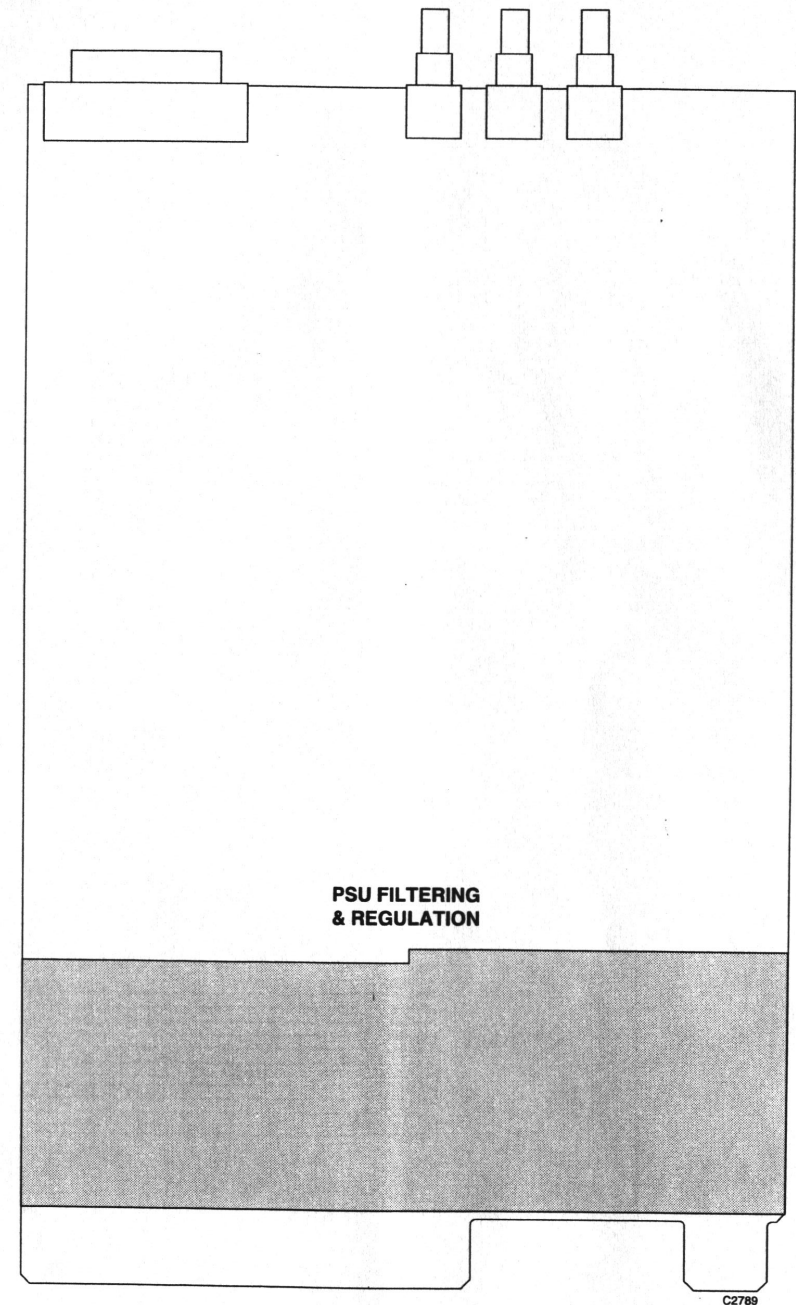


Fig. 7-49 AB1 Control board: Sheet 7 component locations

PSU filtering and regulation AB1

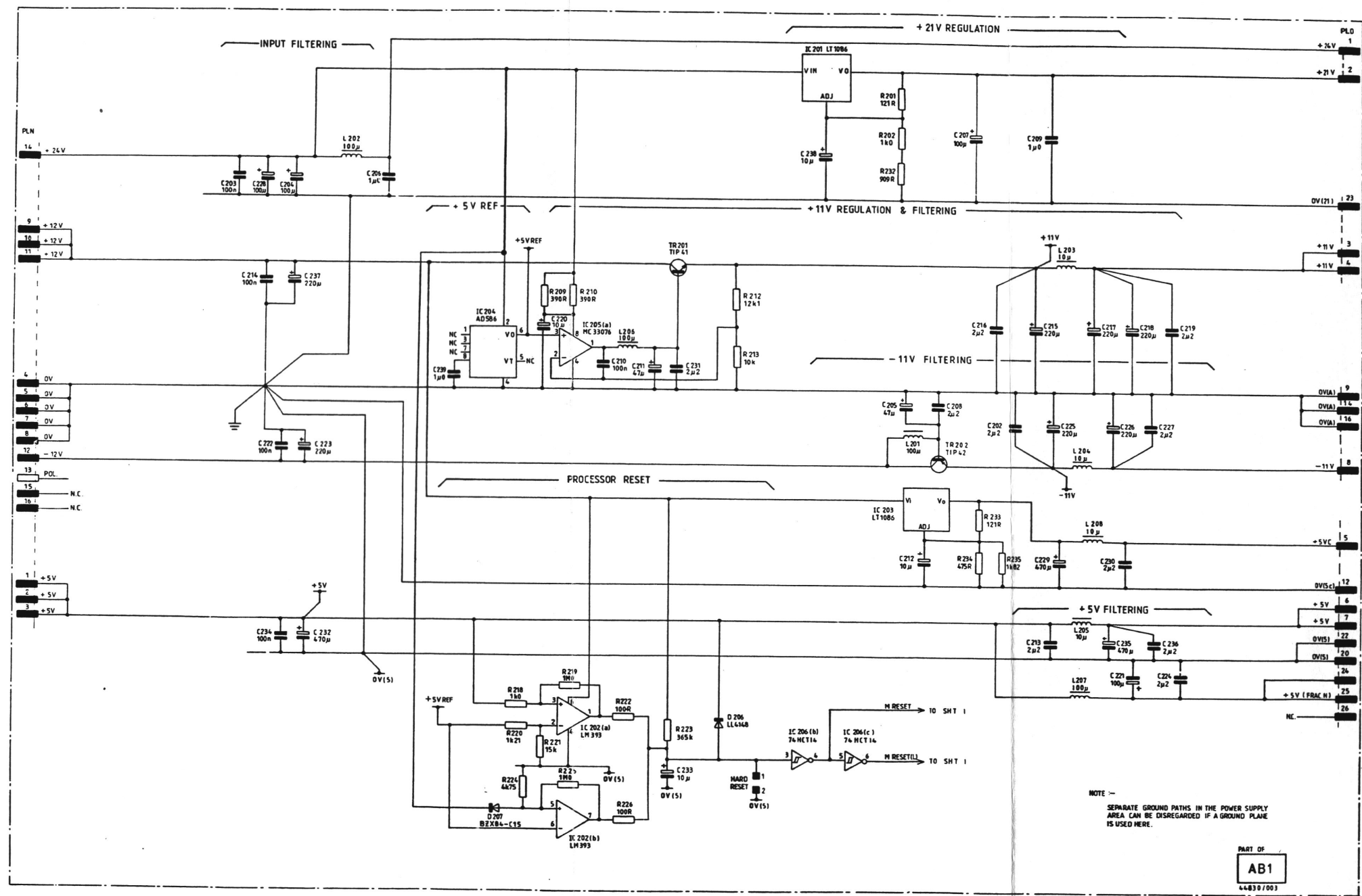


Fig. 7-50 AB1 Control board: PSU filtering and regulation circuit

PSU filtering and regulation AB1

Power supplies AB1

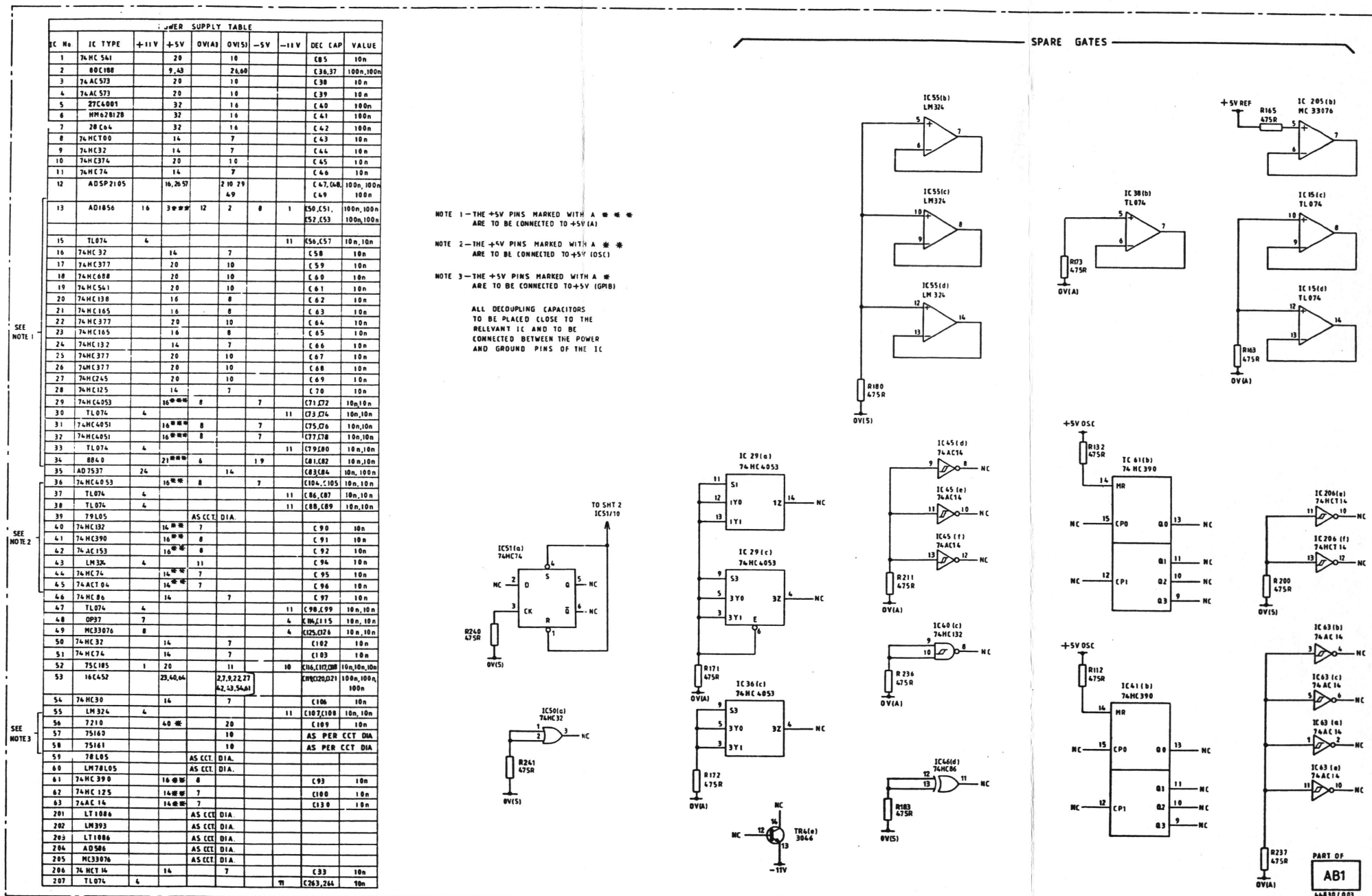
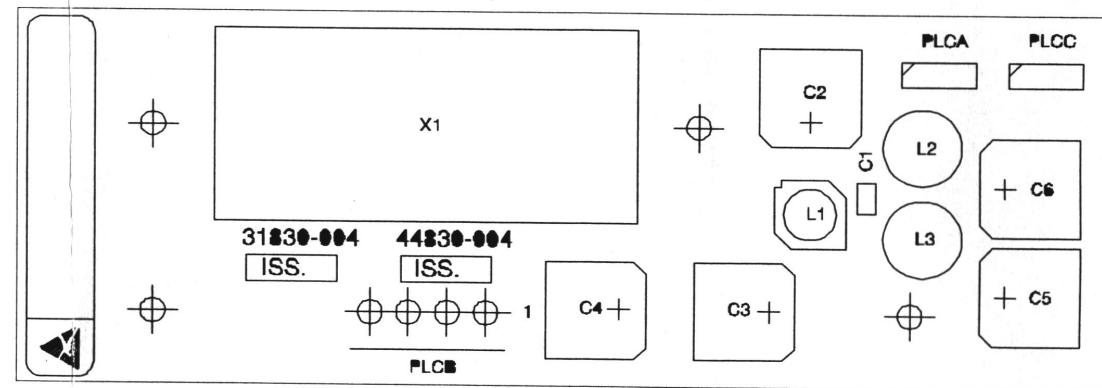


Fig. No. Z44830/003X Sheet 8 of 8 (Issue 4)

Fig. 7-51 AB1 Control board: Power supplies circuit

Component layout **AB1**



Power supplies AB1

Backlight inverter board AC1

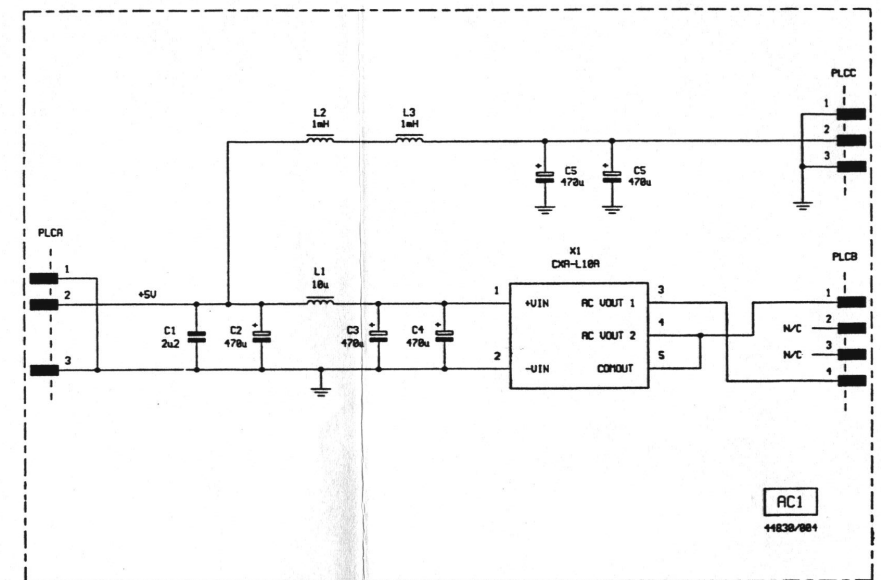


Fig. 7-53 AC1 Backlight inverter board circuit

Backlight inverter board AC1

Keyboard AF1

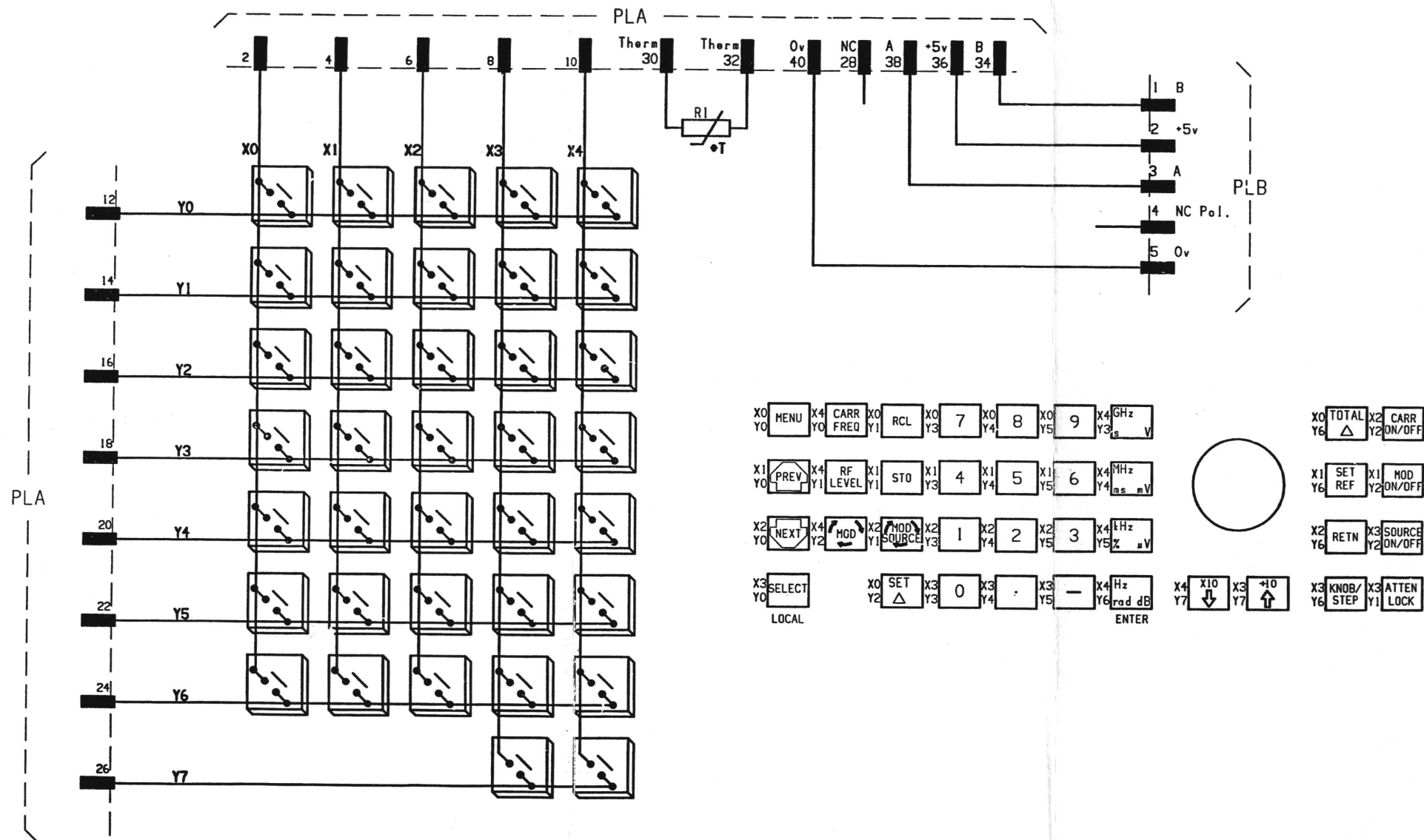
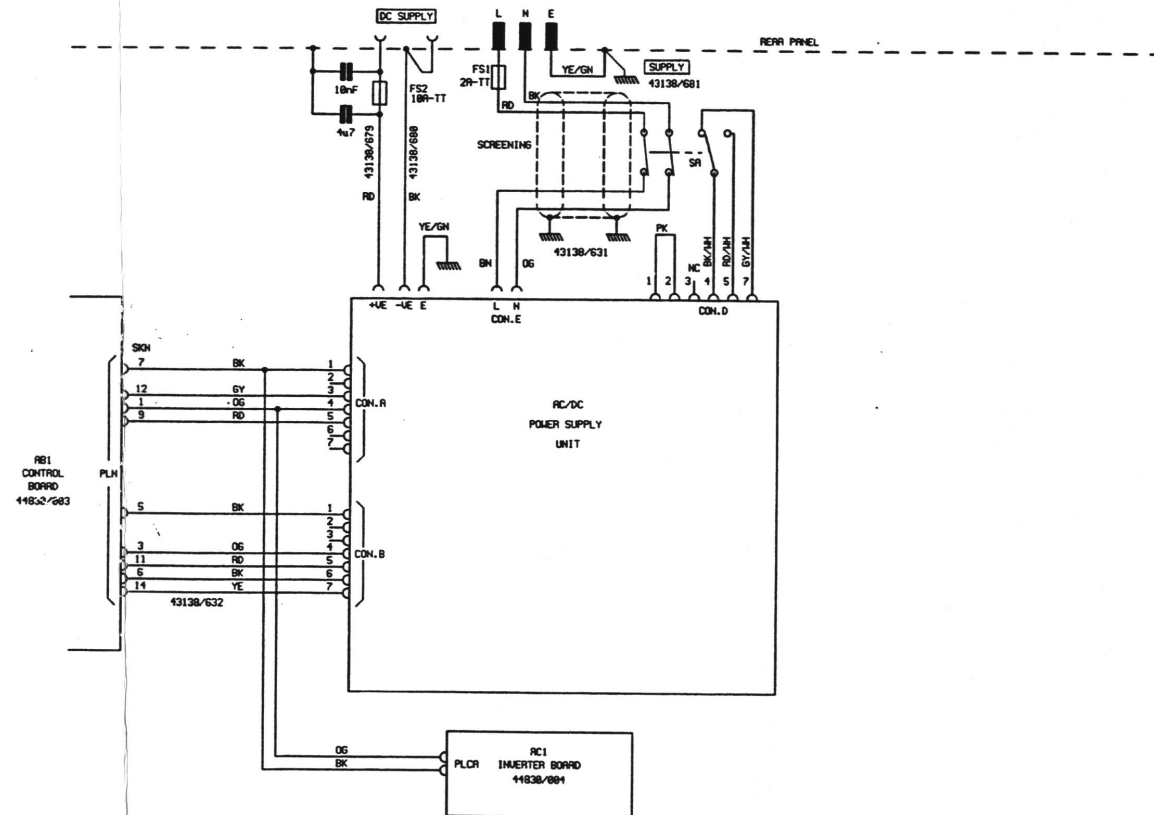


Fig. 7-54 AF1 Keyboard circuit



Keyboard AF1

AC-DC input

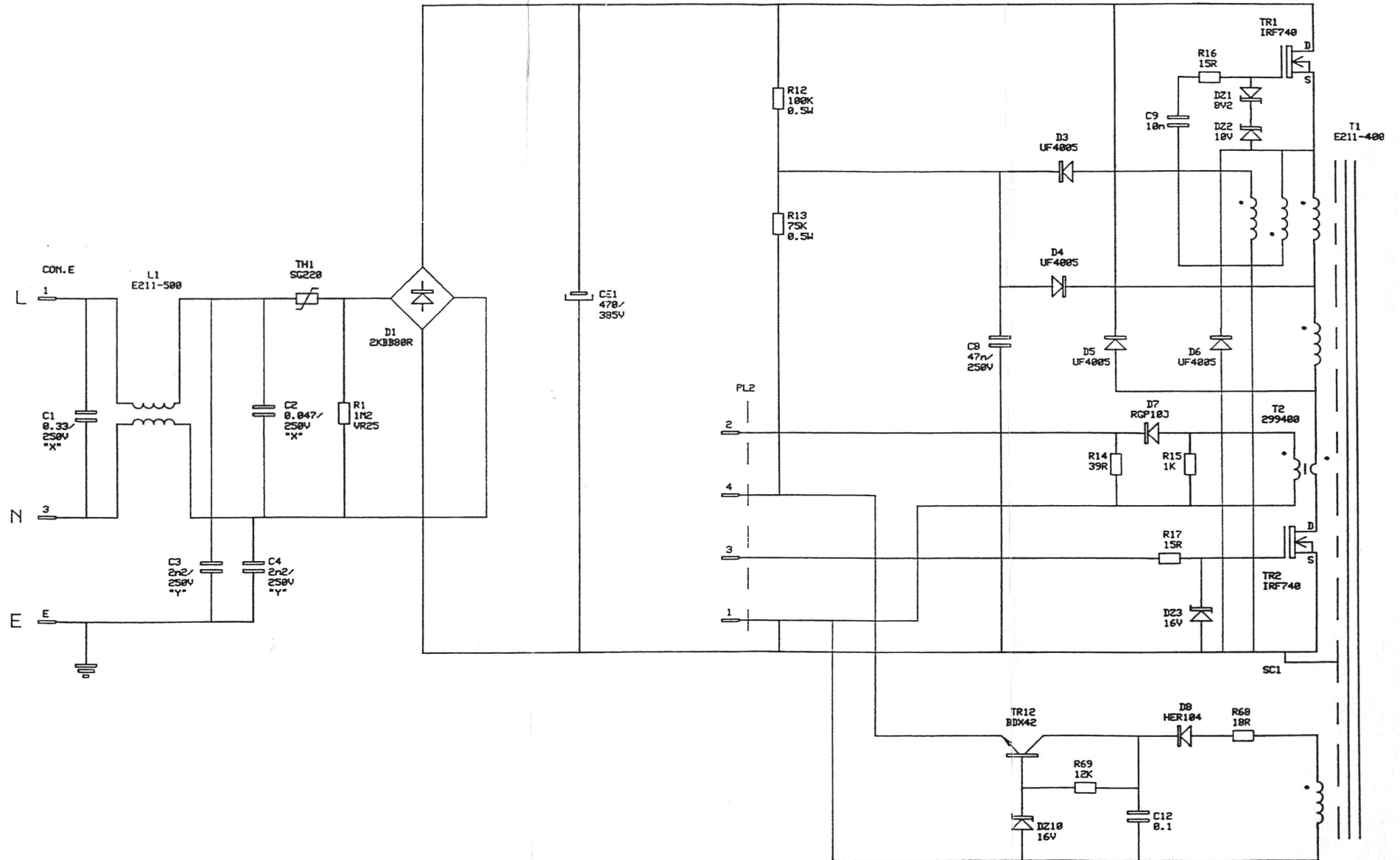
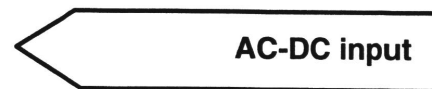


Fig. 7-56 AC/DC supply: AD-DC input circuit

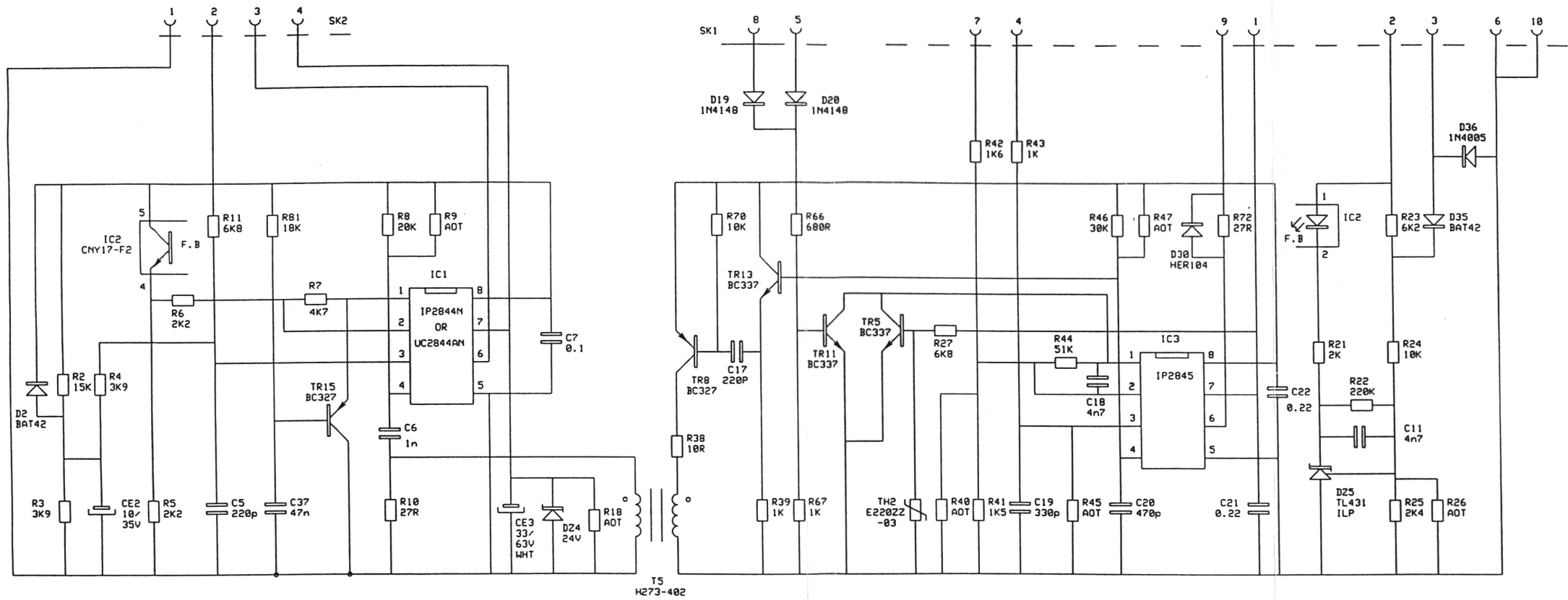
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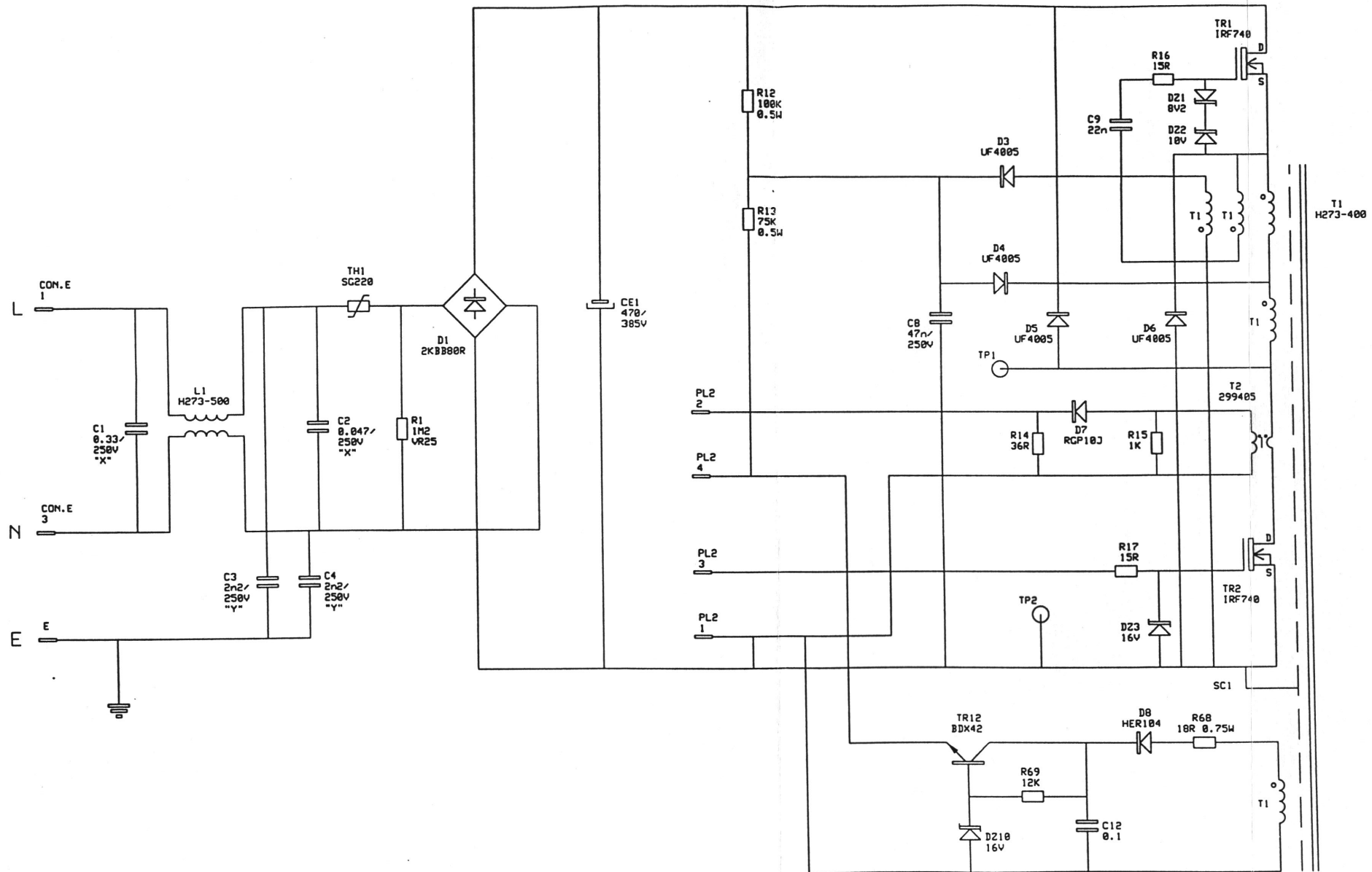
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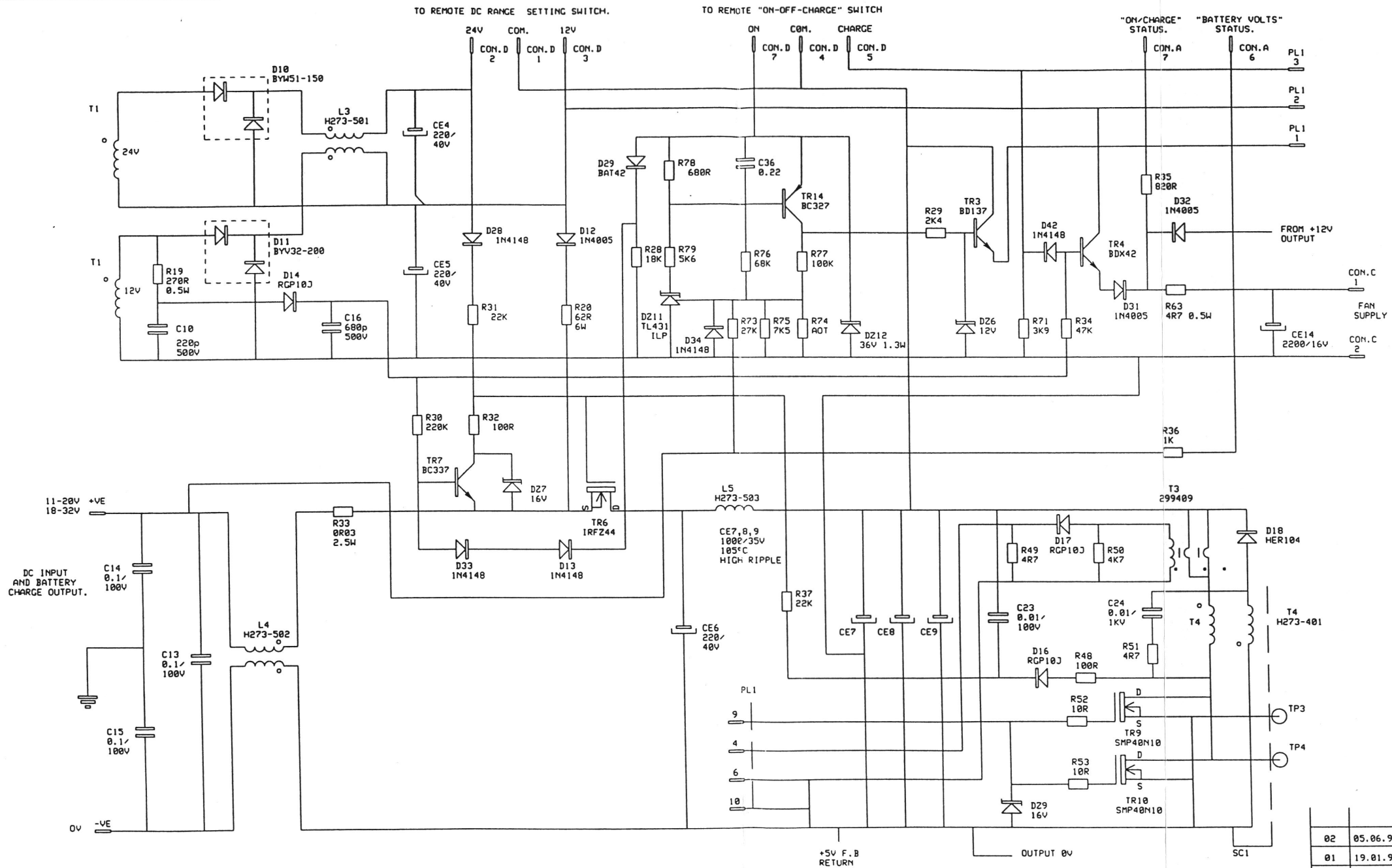
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CIRCUIT DIAGRAM.

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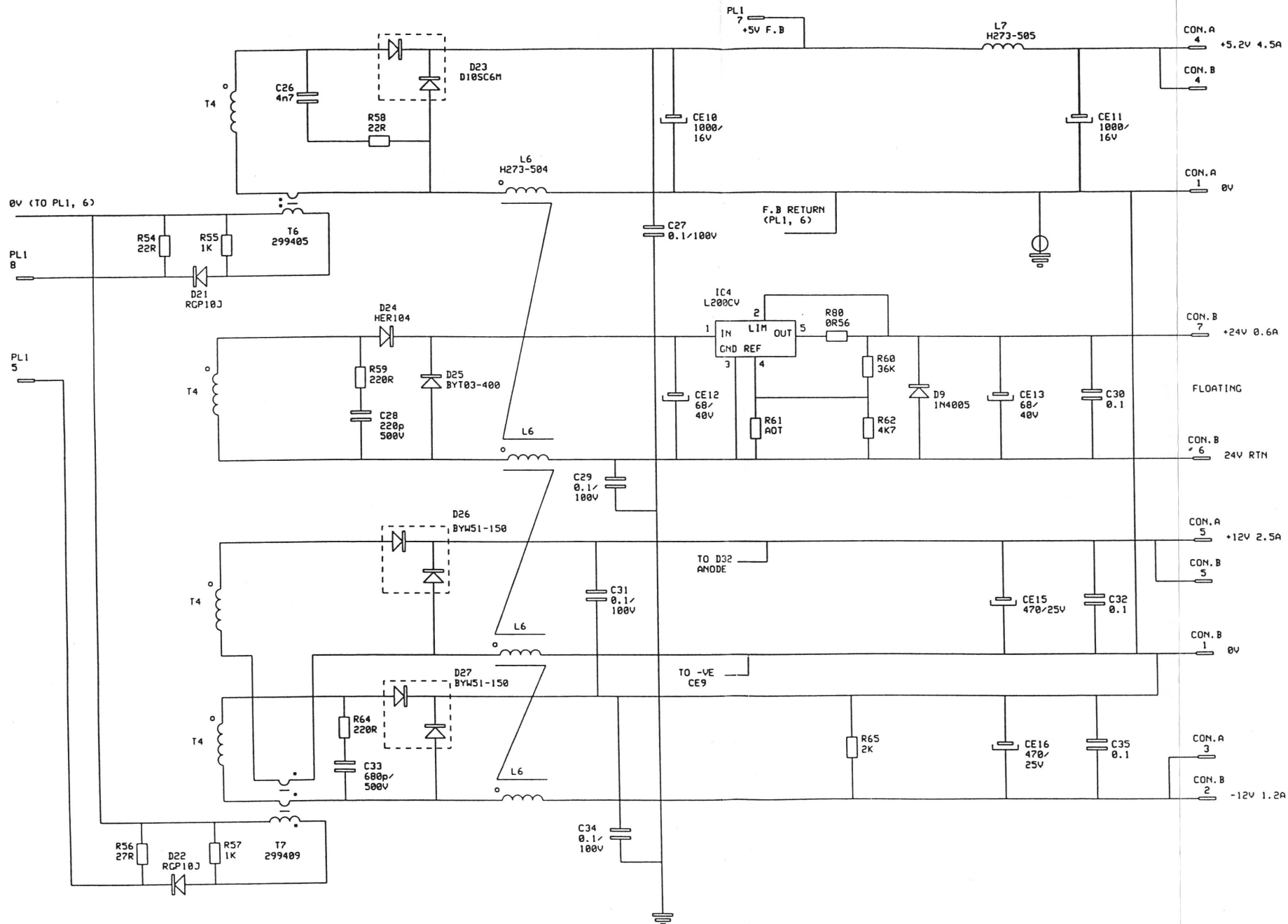
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ISSUE	DATE	MOD.	APPVD.



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ISSUE	DATE	MOD.	APPVD.

DC-DC input

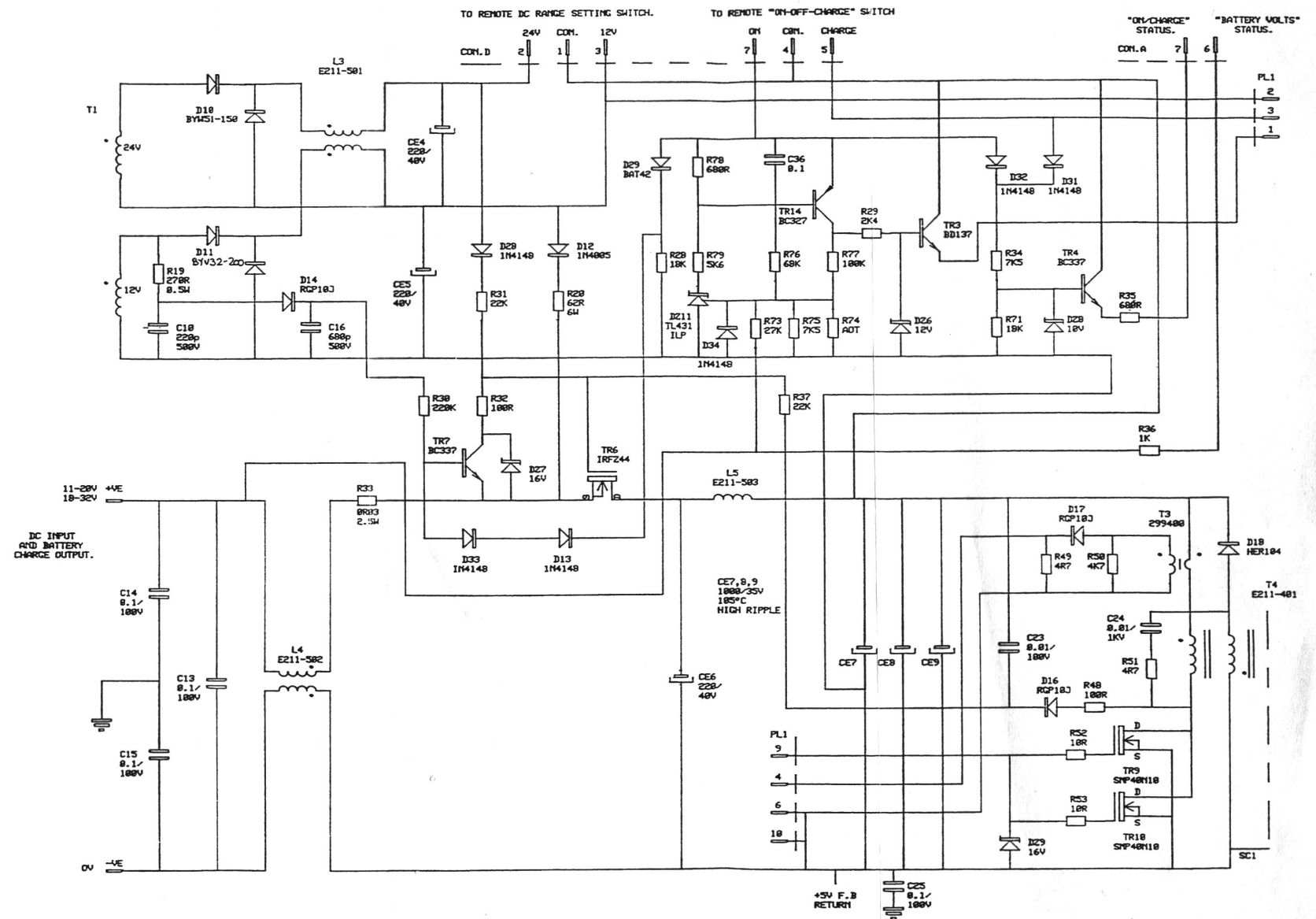


Fig. 7-57 AC/DC supply: DC-DC input circuit

DC-DC input

Control

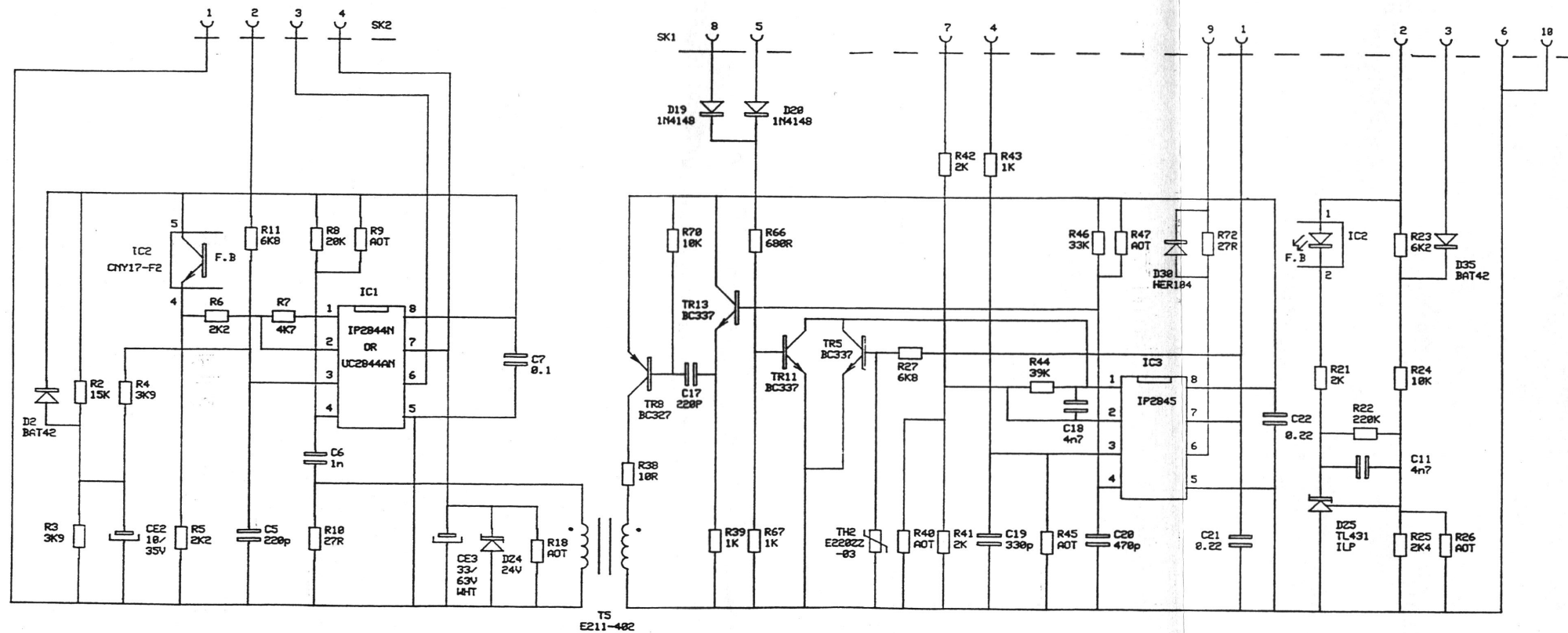
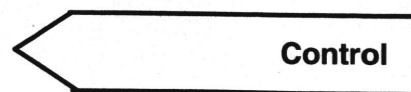


Fig. 7-58 AC/DC supply: Control circuit



DC output

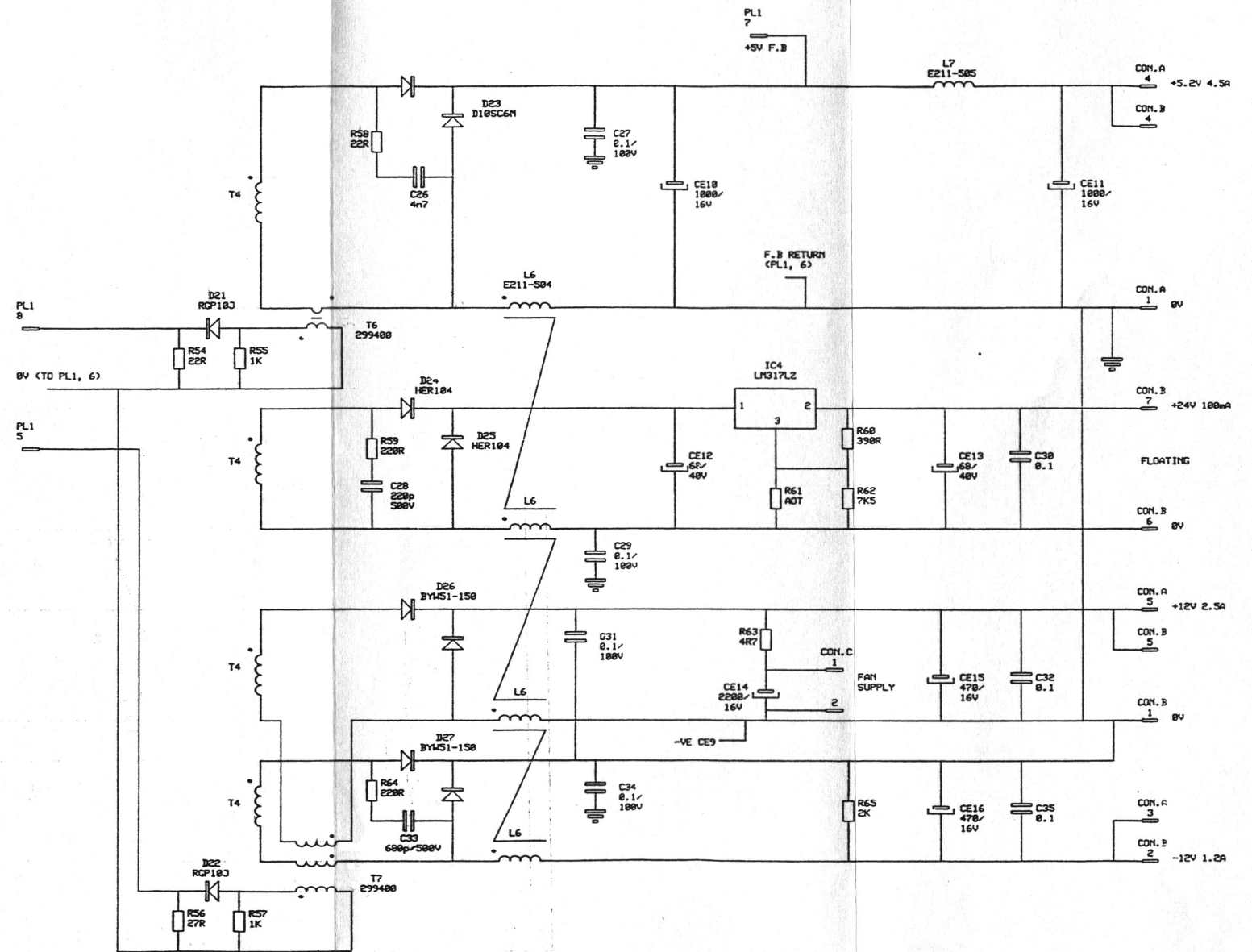


Fig. 7-59 AC/DC supply: DC output circuit

DC output